

A GRAY TO BINARY TRANSLATOR AND SHIFT REGISTER

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The purpose of this report is to describe the theory and operation of a combined Gray (reflected binary) to binary code translator and shift register. The Gray or "Reflected Binary" code has the unique advantage of presenting only a single digital change at the transistion of one quantum step to the next. Translation of the Gray code output to binary code is required as computing and decoding in Gray code are not possible by the usual binary circuit configurations. Gray code computing circuits can be devised, but each of such circuits would require some system of operation on the Gray code similar to the translation process.

Translation Process

Although it is possible to describe the arithmetical gymnastics which show the required translator process, it is simpler to describe here the basic process by the comparison of the representative groups of Gray and binary numbers shown in Figure 1. Only 4 digits are shown in the Figure; the general rules apply, however, to any number of digits. In examining the two different codes it is readily seen that the most significant digits of the codes are slways the same in equivalent numbers. In the example shown in Figure 1 the first translation step shows the most significant digit (#1) becoming binary without change. The next or 2nd digit of the binary number depends, however, on the comparison of the 2nd Gray digit and the 1st binary digit. If in this comparison the digits are alike (0,0, or 1,1) the resulting binary digit is a 0; if they are different (0,1 or 1,0) the resulting 2nd binary digit is 1. In turn, the 3rd binary digit depends on the same comparison of this resulting 2nd binary digit with the 3rd Gray digit. When these comparisons have been completed down to the least significant digit, the result is the equivalent binary number.

A basic functional configuration for translation of parallel Gray code is shown in Figure 2. Here the NOT AND gates provide the series of comparisons described above. The NOT AND gate is a device such that if either one, and only one, of the 2 inputs is stimulated with 1, the output will be a 1. If both or neither are stimulated, the output is a 0. The

connections to these gates are such that the nth binary digit is the result of the NOT AND comparison of the nth Gray digit and the (n+1) th digit resulting from a similar previous comparison. It is apparent that the binary input to the NOT AND gate is delayed with respect to the Gray input from the encoder by the time required for the previous comparisons of the more significant digits. The NOT AND gate must therefore be capable of comparing two input pulses that are not necessarily coincident.

Figures 3 and 4 show how these two methods of translation may be used in an Optical Data Transmitter System. In the serial method of translation of Figure 4 the two directional shift register is required to reverse the transmitter sequence to least significant digit first, this being necessary for the serial addition of aprallax correction. The requirement of this additional register appears to outweigh the advantages of using the simpler serial translator. Methods for translations of the parallel code were therefore primarily considered.

NOT AND Gate

In a previous report* there is discussed the problems of NOT AND gates for input signals which are not exactly coincident. In his report several types of transistor and diode NOT AND gates were shown which are applicable to a parallel code translator. Investigations of the shift register circuits, however, showed the possibility of combining the functions of translator and shift register, reducing the total number of components required for these two functions. This resulted in a program controlled NOT AND gate configuration shown in Figure 5. The essential parts of this gate are the "one bit" register of the shift register** and a supplementary threshold 2 AND gate. As indicated in this figure, steering control has been added to register #2. The function of the steering control is to control input pulses in such a

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*Anticoincidence or 'Not And' Gate", by L. W. Hussey.

**"Storage and Addition of Binary Numbers", by J. R. Harris.

way that they always change the state of the register. That is, if the register is in a state of 1, a pulse on the input will change it to a 0; if the state is a 0, a pulse will change it to a 1. This action is identical to the count action of a binary counter stage.

To examine the operation of this gate, assume that both registers have been cleared by a previous operation and that a new pair of digits is read into the register states by setting those stages to one where the digit is a "1" and leaving the other stages in a zero condition. A "compare" pulse is then applied to one of the inputs of the AND gate. This gate is connected to register #1 in such a way as to transmit the compare pulse only if register #1 is in a 1 condition. If the gate does transmit a pulse, it will then change the stage of register #2. The final state of register #2 is the NOT AND comparison of the original numbers. This can readily be checked by trying the four possible combinations: 0,0 and 1,1 which result in a 0; and 1,0 and 0,1 which result in a 1. A desirable feature of this gate is that the input signals to be compared do not have to be coincident. The only timing requirement is that the registers be set before the "compare" pulse is applied.

Figure 6 shows the configuration for a parallel Gray to binary translator incorporating this NOT AND Gate. Each register stage is also a part of a complete shift register, the connecting circuits of which are not shown for reasons of simplicity. To examine the translation operation assume that the shift register has been cleared initially so that all "One bit" registers are in a state of 0. Under the control of the system program a Gray code number is "read" in the encoder and the digits, in short duration pulse form, are applied to the inputs of register. When the condition of the register has stabilized, storing this parallel Gray code number, a "translate" program pulse is applied at AND gate #1. The NOT AND comparison described above is then made for the most significant digit in register #1 and the next digit in register #2. The resulting condition of register #2 is the binary equivalent of the original Gray digit. After a time delay of sufficient length to insure translation and stabilization in register #2 the translate pulse is applied to gate #2, comparing the state of registers #2 and #3. After this comparison, the digit in register #3 is in binary form. Again, after an appropriate

delay the translate pulse is applied to gate #3 with the result that all registers are then storing the binary equivalent of the original Gray number.

Circuits

Figure 7 shows in schematic form the details of the translator described above. For simplicity, only 3 storage registers are shown and the interstages for digit shifting are omitted. The circuit for the storage register has been previously described*.

The method for steering control for this register is shown in Figure 4.1-9. In this figure assume transistor #1 of the register is in the "on" condition, in which case its base and collector are at approximately -10 and -12 volts respectively. The difference between these voltages, 2 volts, is the effective back voltage on diode #1 of the steering circuit. At the same time the base and collector of the "off" transistor are -4 and -35 volts respectively, biasing diode #2 approximately 31 volts in the back direction. It is apparent that under these conditions a positive input pulse on the control circuit, having an amplitude between 20 and 35 volts, would be readily steered through diode #1 to the base of transistor #1, turning this transistor off and transistor #2 on. The storage effect of C_1 and C_2 tends to keep the input pulse correctly steered until the register has completely changed state. After several time constants of R_1C_1 (or R_2C_2) diode #2 becomes the readily conducting diode to an input pulse, enabling the next input pulse to turn transistor #2 "off" and #1 "on". The six passive components for the steering control have been packaged into a single functional package, M1751-3, the specifications of which are given in Fig. 13. To provide sufficient triggering level for the register stage a transistor regenerative gate is used for the AND gating function.*

The delays for the translate pulses are obtained from the cascaded stages of regenerative pulse amplifiers in the following manner: at the time the negative program translate pulse is applied, the first regenerative amplifier (amp. #1) is triggered, providing a positive output pulse of about 60 μ sec. duration. The positive leading edge of this pulse is applied to gate #1, while 60 μ sec. later the negative trailing edge triggers amp. #2. The positive leading edge of the output pulse of amp. #2 is applied to gate #2; while an additional 60 μ sec. later amp. #3 is triggered by the trailing edge. This action continues along the entire chain of amplifiers, providing in each step a delay of approximately 60 μ sec.

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*"Storage and Addition of Binary Numbers", by J. R. Harris.

As seen in the diagram of Figure 7, the output of the regenerative amplifier is differentiated and attenuated from approximately 25 volts to 20 volts by the condenser divider network, C_1 and C_2 , providing the proper critical triggering level for the regenerative gate. When the regenerative gate is triggered, the emitter current maintaining the transition of the gate in the "ON" condition is supplied by the charge stored in C_1 and C_2 . C_1 and C_2 in parallel, therefore, determine the charge available in the output pulse of the gate. In determining the value for the parallel combination of C_1 and C_2 two things must be considered. If the register controlling the regenerative gate has just changed state due to the translation of the digit it was storing, the change must be applied to the gate before translation of the next digit by charging C_1 and C_2 in parallel through R_1 . The higher the value of C_1 , plus C_2 , the greater the time required per digit for translation. Yet C_1 and C_2 must be sufficiently large for the gate to supply an adequate signal charge for setting its associated register stage. As high speed translation was not required in this system it was possible to make C_1 plus C_2 large enough to meet this requirement. Where higher speed translation may be required a non-storage type gate might be used in conjunction with regenerated gain.

The dotted enclosures on Figure 7 indicate the functional packages used in the translator. References to their specification are given in Table 1.

Digit Shifting Register

In a report previously referred to* there is described various configurations for digit shifting registers. One of these types is shown functionally in figure 9. In this diagram, it is seen that the program shift input is applied simultaneously to all the interstage threshold 2 AND gates and the zero set input of register #1. The first shift pulse, therefore, sets register #1 to zero and enables one of the two AND gates in all the interstages. That AND gate which is enabled is determined by the original state of the register just ahead of the interstage. The delay provides the memory of this state even though the controlling register may already be in a changing condition. Therefore, if register #1 was in a state of 1 just before the first shift pulse, the gate on the set 1 lead of register #2 is enabled, setting the register to 1 if it was a zero or leaving it in a state of 1 if it was a 1. Likewise, the state of register #2 is transferred to register #3 and the state of register #3 to a following stage at the time of the first shift pulse. In effect, the original number stored in the register is shifted one digit to the right. Successive shift pulses perform the same operation, each pulse shifting the stored number one digit to the right until all

 *"Storage and Addition of Binary Numbers", by J. R. Harris.

digits of the number have been shifted out of the register. As the shifting process for this type of register is entirely controlled by program pulses, the interstages cause no interference with the translation process. In the actual shifting circuit used for the combined translator-register circuit, the first two stages of which are shown on Figure 10, the delay and gating functions are accomplished with a simple R, C, and diode network, identical with the steering control network for the translator. The connections to the registers differ, however, in that the steering of the input pulse is controlled, not by the same register condition, but by the adjacent register. Successive shift pulses, therefore, transfer the states of one register to the adjacent register, providing the digit shifting process described above.

The loss through the interstage is small enough that the registers may be set directly from the shift driver output without the additional interstage gain indicated in the functional diagram, Figure 9. Seven register stages have been operated from one M1733-1 driver satisfactorily. For a full 15 digit system, it is expected that the register load would be divided between 3 such driver stages.

Packaged System

The translator-shift register was assembled using the functional packages developed under the packaging program. The complete interconnecting schematic for this system as used for demonstrating the operation of the Optical Encoder is shown in Figure 11, together with component values and tolerances not covered by the package specifications. In this demonstration model for the six digit optical encoder a 7th bit-storage register (Register A) was used, corresponding to the modulator gate for an actual data transmitter system. The oscilloscope indication of the output of this register represented the envelope coded signal output of a data transmitter system.

The control program sequence for the demonstration model is shown in Figure 12.

Here it is seen that the reading of the code in the optical encoder and the storing and translation of the code in the register are performed during the 1667μ sec. time slot before the first digit is to be transmitted out of the system.

Overall system specifications for the translator-register and the individual package specification references are given in Table I of this report.

Conclusion

For an optical encoder with requirements based on a typical data transmission system the presented configuration of circuits for code translation and digit shifting appears to be the simplest from the standpoint of the number of active components required. The model constructed for use with the 6 digit encoder has operated satisfactorily for over two months and has been demonstrated many times during that period. Although rigorous life tests have not been made on the overall system, such tests are being made on the **individual** components package. From the statistical results of **these tests**, the performance of the overall system can be resolved.

The feasibility of encoding by optical means was proved with the demonstration of the 6 digit optical encoder. Its demonstration with this translator-shift register proves the practicality of optical encoding in a data transmission system.

TABLE I

Requirements for 6-digit Translator-Shift Register System

<u>Power Supply</u>	<u>Voltage</u>	<u>Tolerance</u>	<u>Current</u>	<u>Power</u>
	+40	± 5 v	80 ma	3.2 watts
	-45	± 5 v	80 ma	3.6
	-10	± 1 v	1 ma	.01
	-150	± 25 v	2 ma	<u>.3</u>
			Total	7.2 watts

<u>Program Input</u>	<u>Pulse Amplitude</u>	<u>Pulse Length</u>	<u>Input Impedance</u>
Translate	-3 v min.	1 u sec. min.	5000 ohms
Shift	-3 v min.	1 u sec. min.	1000 ohms
Encoder			
Set "1"	+10 v min.	5 u sec. min.	1000 ohms

GRAY	DECIMAL	BINARY
0000	0	0000
0001	1	0001
0011	2	0010
0010	3	0011
0110	4	0100
0111	5	0101
0101	6	0110
0100	7	0111
1100	8	1000
1101	9	1001
1110	10	1010
1111	11	1011
1010	12	1100
1011	13	1101
1001	14	1110
1000	15	1111

DIGIT 1 2 3 4

1101
1001
1001
1001

Fig. 1 Comparison of Gray and Binary Codes

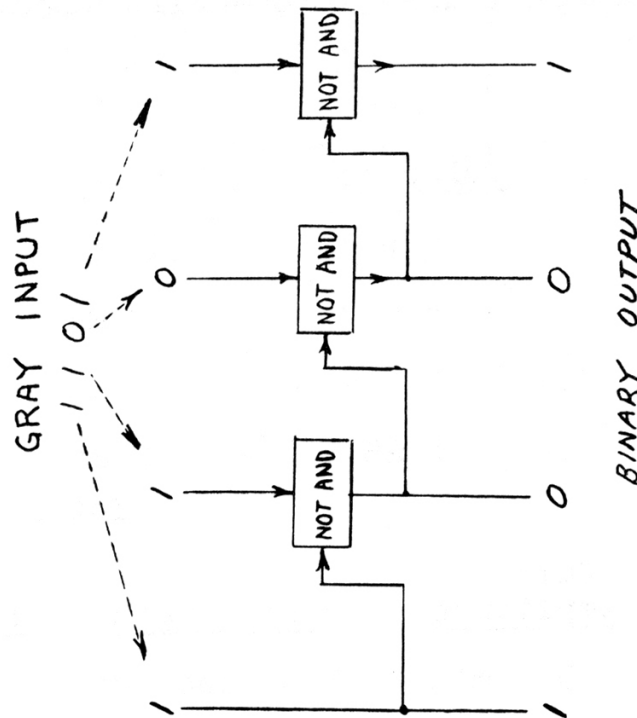


Fig. 2 Parallel Translation

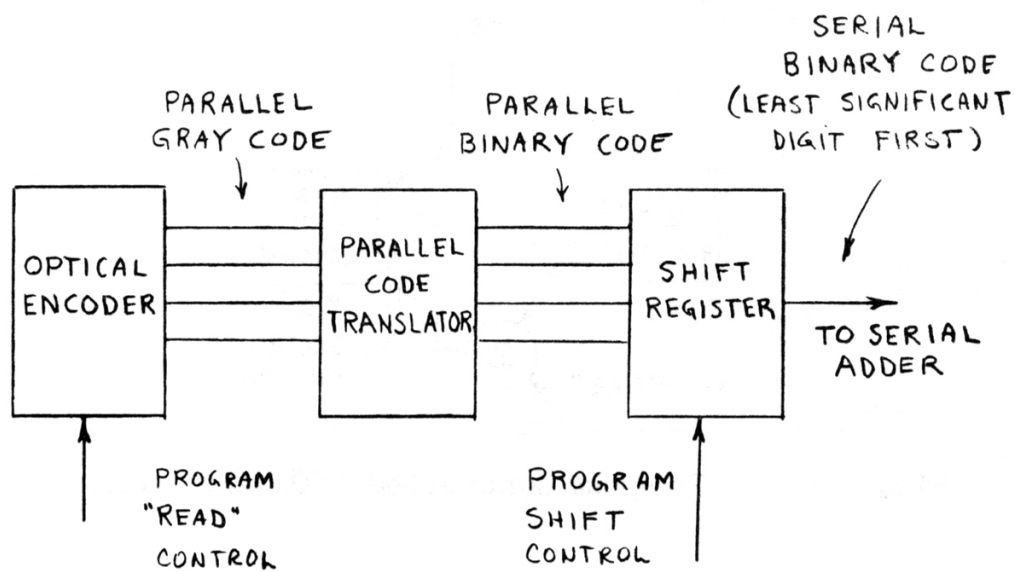


Fig. 3 Optical Data System Using
Parallel Translation

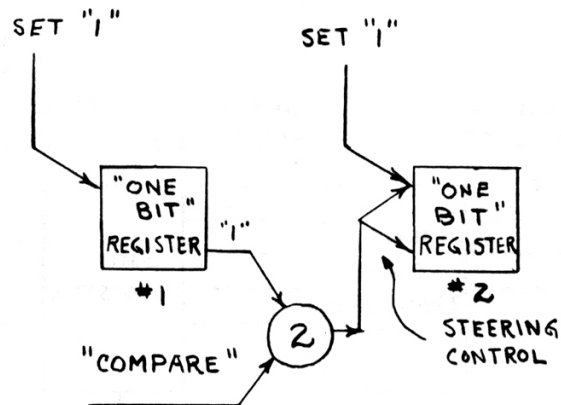
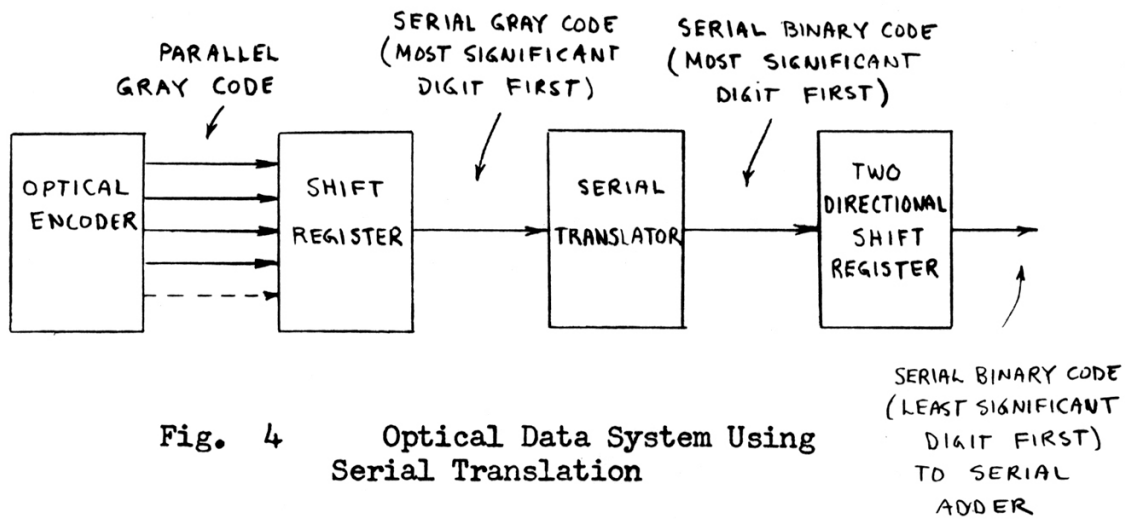


Fig. 5 Program Controlled "NOT AND" Gate

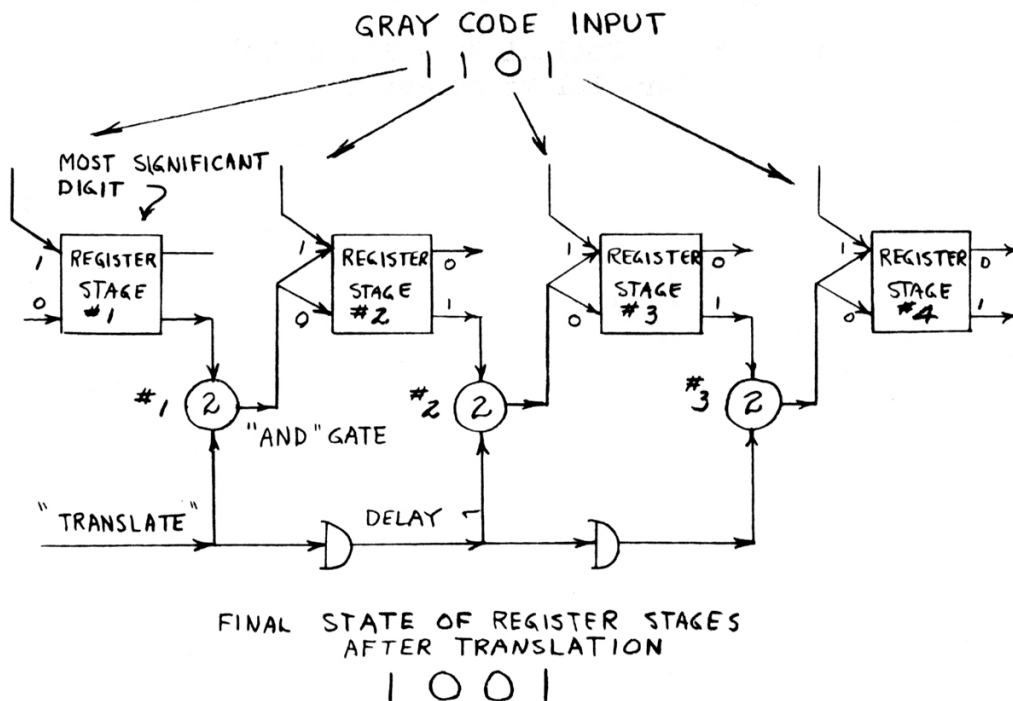


Fig. 6 Functional Schematic of Gray to Binary Translator

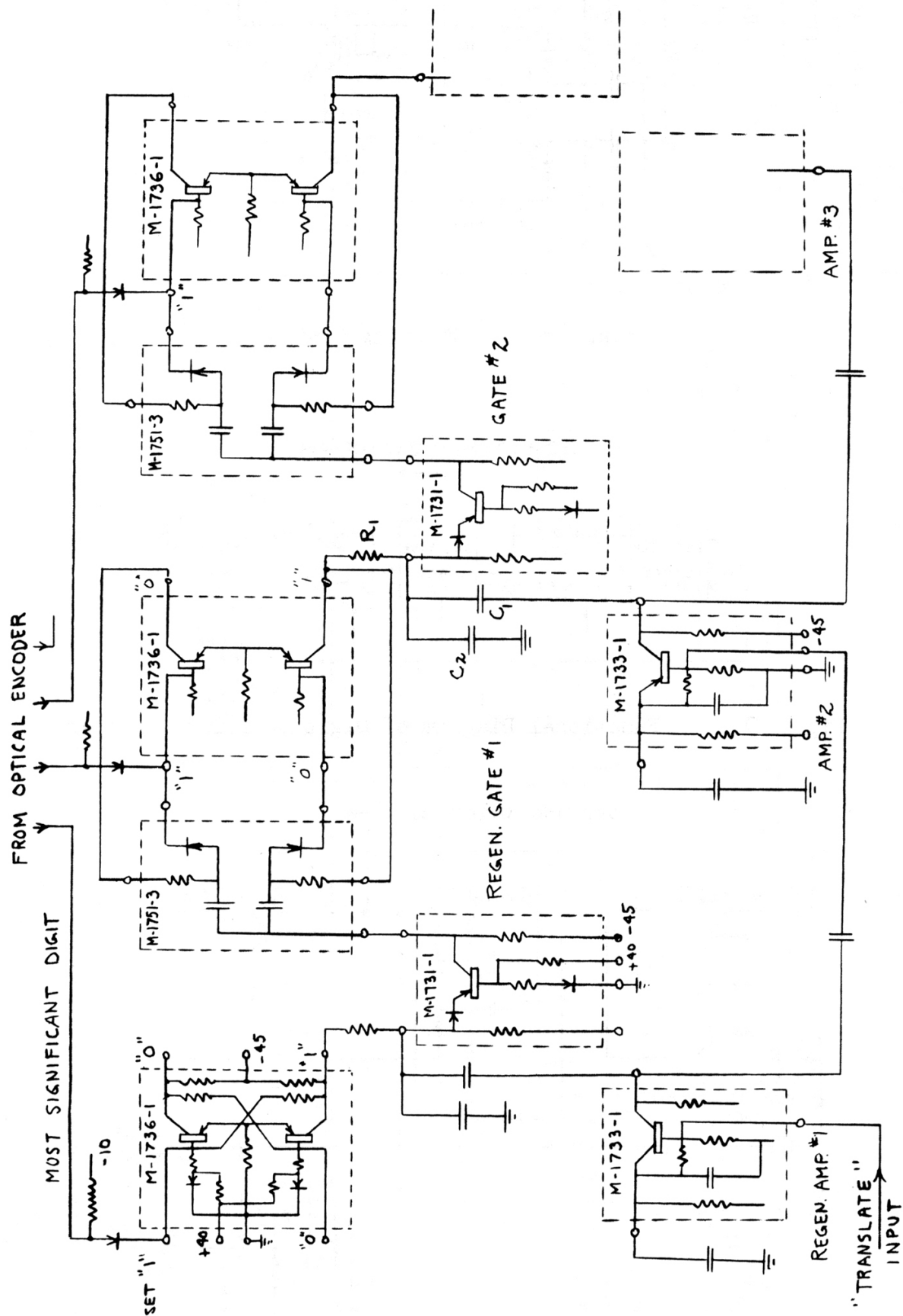


Fig. 7 Partial Translator Schematic

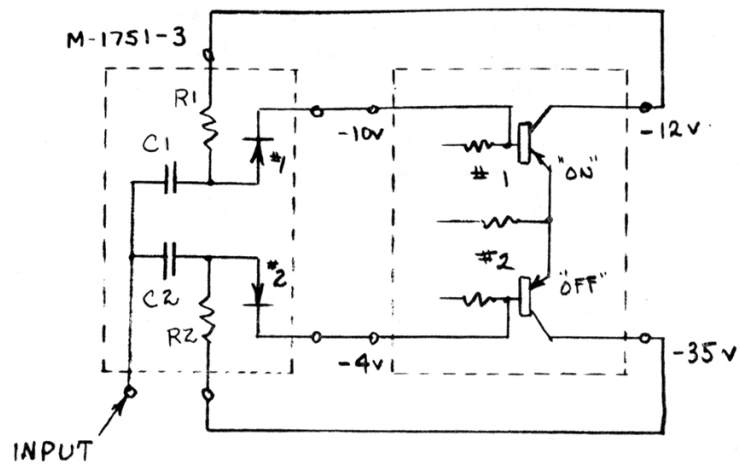


Fig. 8 Steering Control

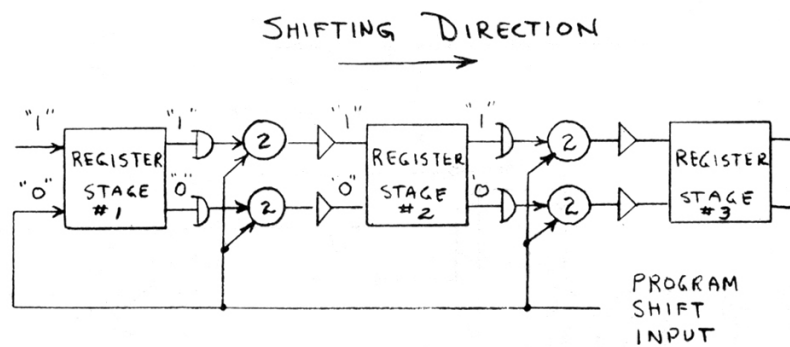


Fig. 9 Functional Diagram of Digit Shifting Register

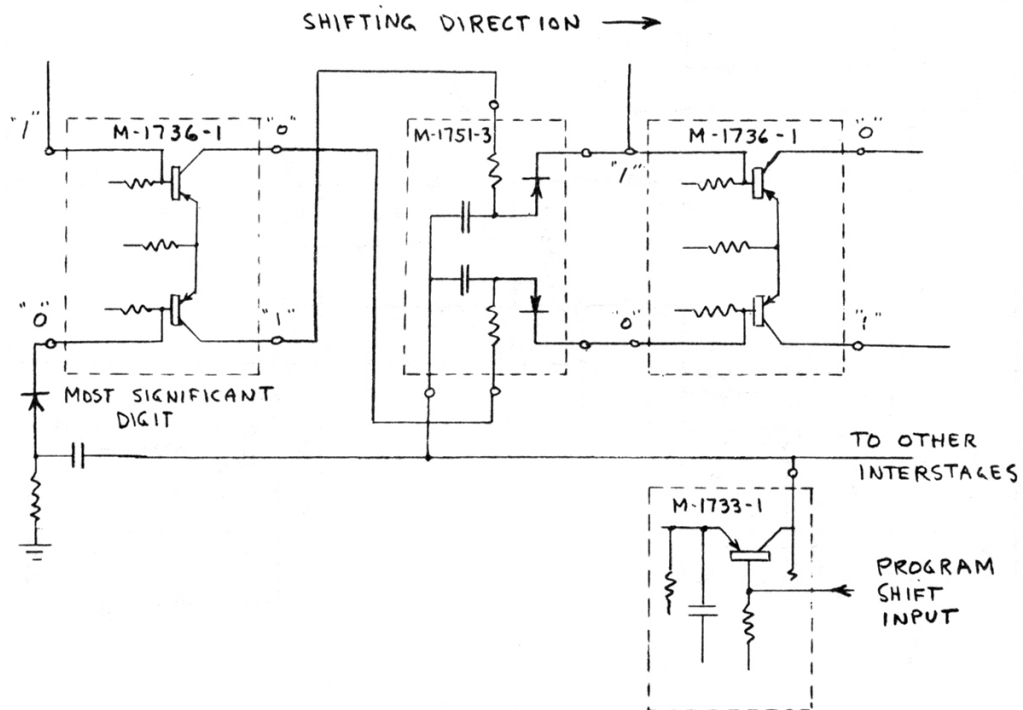


Fig. 10 Digit Shifting Register Schematic

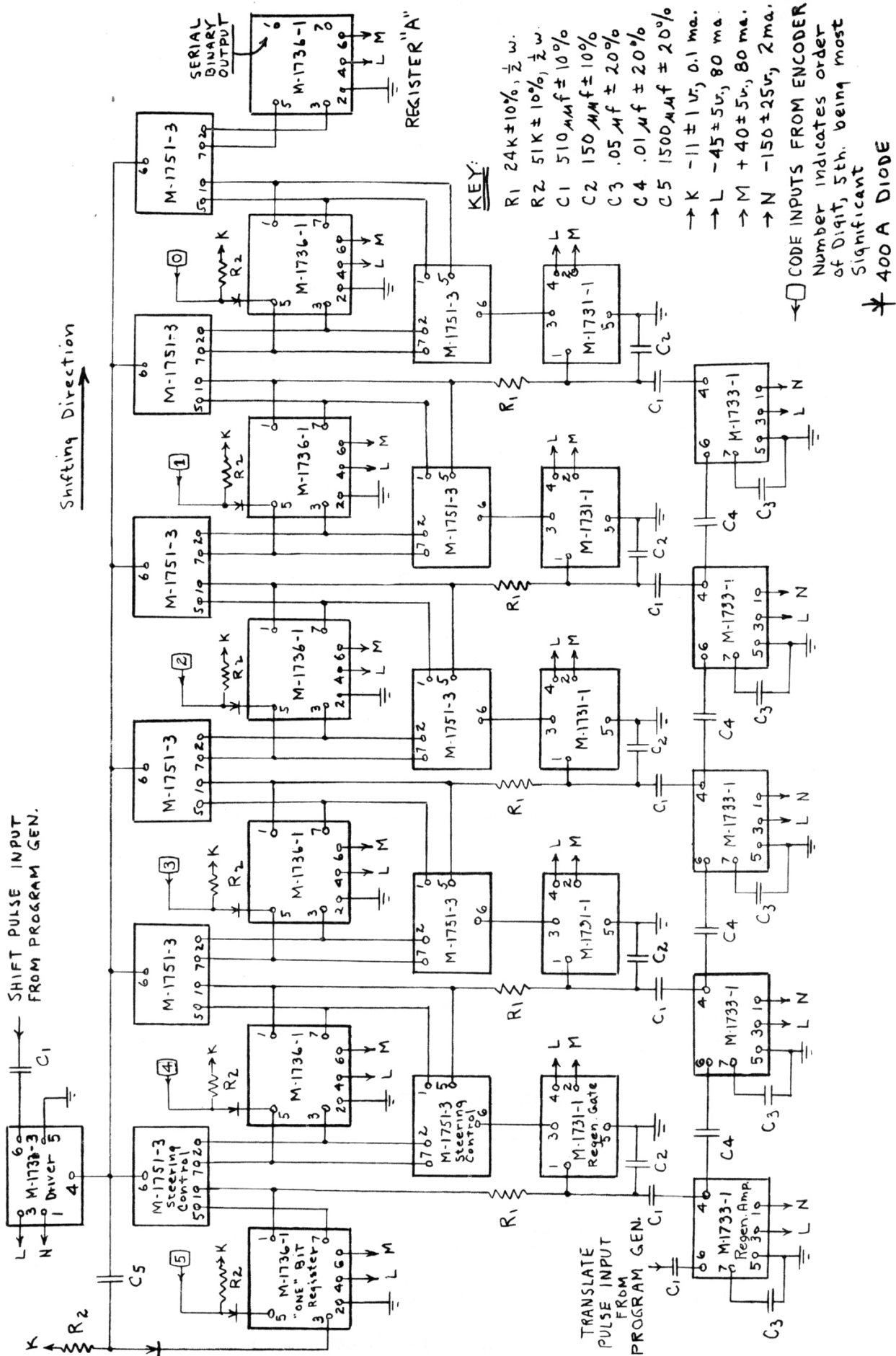


Fig. 11 Translator-Shift Register Schematic

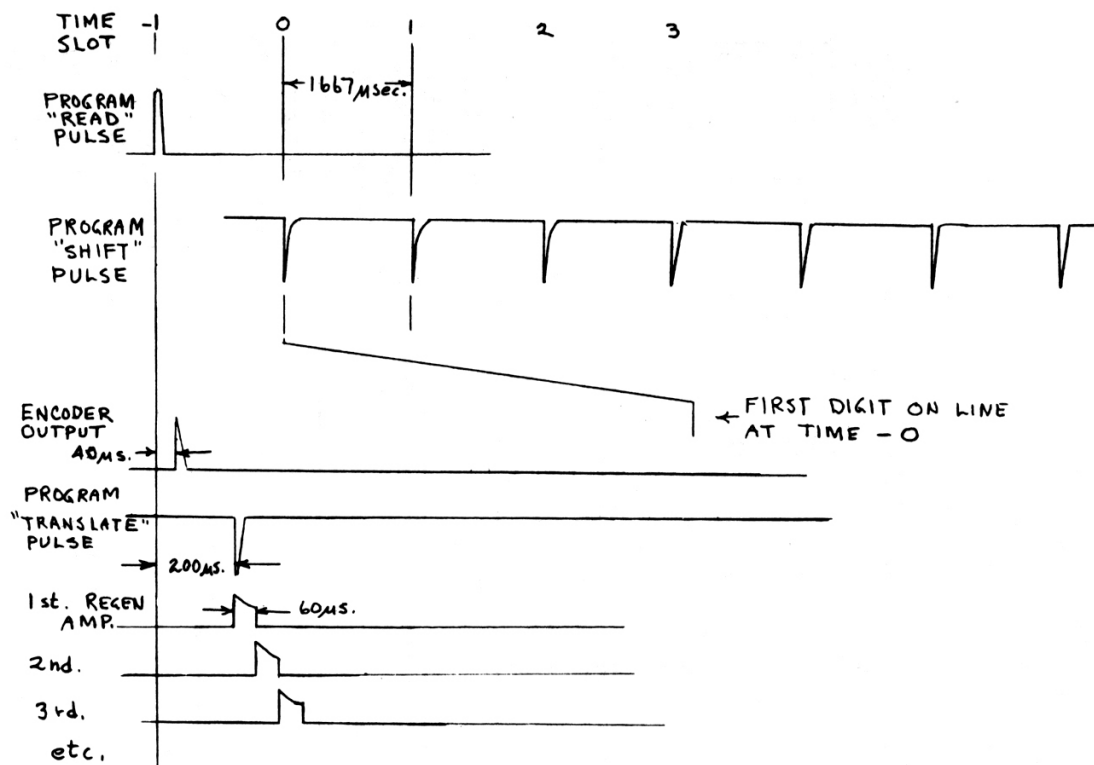
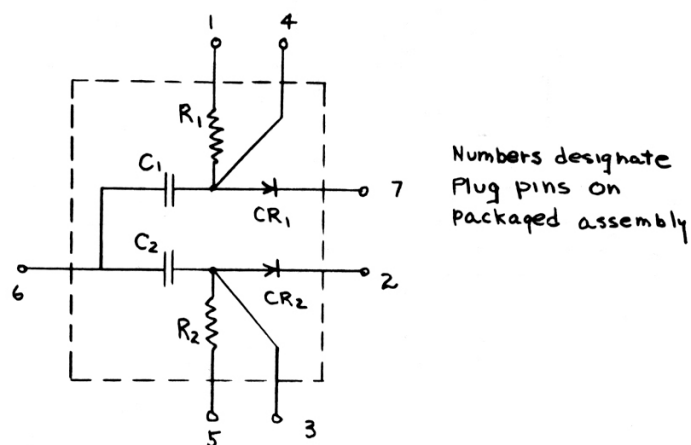


Fig. 12 Translator-Shift Register Programming



R_1, R_2 51 K $\pm 10\%$ Allen Bradley - $\frac{1}{2}$ w.
 C_1, C_2 1500 μ f $\pm 10\%$ ERIE GP2B
 CR_1, CR_2 400A Diode

Post-Potting D.C. Resistance Tests

5 to 3	51 K $\pm 20\%$
1 to 4	51 K $\pm 20\%$
6 to 3	Open Circuit
6 to 4	Open Circuit
3 to 2	(Forward) 1.0 volt drop max. at 2.0 ma.
2 to 3	(Back) 500 k min. at 20 volts
4 to 7	(Forward) 1.0 volt drop max. at 2.0 ma.
7 to 4	(Back) 500 k min. at 20 volts

Fig. 13 M 1751-3 Diode Control Package Specifications

N O T E S O N T H E
D E S I G N O F H I G H S P E E D D I G I T A L
C O M P U T E R S U S I N G T R A N S I S T O R S

J. H. FELKER

INTRODUCTION

CATALOG OF BLOCK DIAGRAMS

A TRANSISTOR BLOCKING OSCILLATOR

COUNTING DOWN WITH BLOCKING OSCILLATORS

BASIC TRANSISTOR AMPLIFIER

A WORD GENERATOR

DELAY LINE STORAGE

BIT STORAGE WITHOUT FLIP-FLOPS

A BINARY ADDER

INTRODUCTION

This section reports work that has been done towards a high speed digital computer based on transistors and semi-conductor diodes. Specific components that have been built are discussed. The material is largely a series of independent memoranda written at different times and for separate purposes. This accounts for some of the inconsistencies and the lack of integration that the reader may detect.

1.1 WHAT A COMPUTER DOES

A statement to the effect that a digital computer is a giant brain is a very helpful statement to make when one is trying to get a group of people interested in digital computers. However, once the people are interested, this statement has lost most of its usefulness. If someone really wants to know how a digital computer works, what kind of processes are used by the computer, and what kind of components are in the computer it doesn't do the person much good to say that a computer is a giant brain. Perhaps a better statement to make is that a digital computer is a desk calculator with an operator built in. The operator is a person of very limited resources, very great speed, capable of following very long instructions exactly as those instructions are given, and incapable of doing anything useful not planned when the original instructions were made up.

The arithmetic unit of the computer will be able to do the same kinds of things that a desk calculator can do except that it will be able to do them much faster. It will be able to add, subtract, multiply, divide or perform any other of those numerical operations that can be described in terms of the elementary ones.

As an aid to visualizing the kind of things that a digital computer has to do, it is convenient to imagine oneself faced with a particular problem in numerical computation and see how it could be done on a desk calculator.

Suppose that it is desired to evaluate

$$\int_1^2 \text{Log} (x + \sqrt{\sin x}) \, dx \quad (1)$$

The first step would be to decide how the integration is to be performed. Suppose that it were known that Simpson's rule for integration would give sufficient accuracy for tabulation intervals of 0.05. One would then obtain a large sheet of paper and lay out the computation as on Figure 1. In column A, the values x are listed. In column B, the sine of the entries in A is tabulated from some table. In column C, the square roots of the entries in B are tabulated after being computed with the calculator. In column D, the sum of A and C is tabulated. In column E, the logarithm of the entries in D is tabulated. This column then contains the value of the integral at intervals of 0.05. Column F contains weighting factors which are used to weight the values before they are summed (these coefficients come from Simpson's rule). The product of column E by F is tabulated in G. The entries in G are then summed and the result, when divided by three and multiplied by the tabulating interval is the desired integral.

It is clear that one of the essential features of computation based on a desk calculator is the large sheet of paper to keep track of computation. The piece of paper stores the program for the computation so that the user can merely "follow instructions" as he operates the calculator and consults tables. The sheet of paper also serves as a storage or memory medium for intermediate results.

An automatic computer, which is what we usually mean by a digital computer, must have not only the arithmetic unit corresponding to the desk calculator, but it must have a memory (corresponding to the large sheet of paper) and a control unit (corresponding to the operator).

In distinguishing between an analogue computer and a digital computer it has been said that a digital computer is a computer which has a language. One of the main uses of the language is for instructions. A common instruction scheme is based on the four address code shown in Figure 2. At any

time the control unit in the machine is concerned with four addresses plus an operation instruction. The operation, abbreviated OP, is the arithmetic operation to be performed next. Addresses one and two are the locations in the memory at which the numbers to be operated on are found. Address three is the address at which the result obtained is to be stored. Address four is the address at which the code group for the next step will be found. What takes place in the computer is: The control unit pulls out of memory a four address code. This tells what is to be done in the next step. The machine takes the two relevant numbers out of storage, it performs the indicated operation, it puts the result back into storage in its appropriate place, then it observes the fourth address, looks in that address, and pulls out the details of the next step.

In computer language, numbers are represented as polynomials just as in other languages. Figure 3 illustrates polynomial notation while Figure 4 illustrates that the base need not always be 10. Because electronic apparatus generally has only two states, open or closed, conducting or not conducting, binary numbering systems are used in most electronic computers. Thus only two symbols are admitted, zero and one.

All words or numbers must be stated in terms of their symbols. The control unit of a computer must be able to take sequences (in time or in space) of pulses (ones) and absence of pulses (zeros) and recognize that a certain connection is to be set up. The arithmetic unit must be able to take the same kind of information and do arithmetic. In the next section of this report block diagrams of components for switching, storage, and computing will be presented, while in later sections the specific details of typical transistor designs will be given.

1.2 COMPONENTS

Existing digital computers were, in most cases, built without major effort to control their size. However, concentrated effort on size reduction will be required in order to design a digital computer that will be small enough to compete with the analogue computers now available.

Techniques for miniaturization have been widely developed, but a fundamental difficulty with reduction in the size of components is the problem of what to do with the heat that the components generate. To get really important reduction in size we must reduce the heat generated as well as the size of the components.

The basic reason that digital computers have to dissipate large amounts of power is that they use components that were originally developed for use where power must be developed to drive output devices. A digital computer may go through a million alterations of state before any output device is operated. With this very loose coupling between the internal operations and the output, it is extremely wasteful to perform every internal operation at a power level sufficient to drive an output device. All internal operations in a computer can be reduced to driving a device from one distinct state to another distinct state. If a small digital computer is to be built, it is essential, therefore, to look for components, in which the power involved in going from one state to the other is a minimum. In voltage-operated devices this power is determined by the voltage swing required to change states and the current required to charge up the parasitic capacitances in the available operate time. In current-operated devices the power is determined by the current swing required and the voltage necessary to drive that current through the parasitic inductances in the time allowed for a change of state. As we reduce power dissipation we will be able to reduce size, which will lower the parasitic capacitance and inductance which, in turn, will permit further reduction in power. Not only must the power required to change state be reduced, but so must the power lost in cathode heaters and similar auxiliaries to active devices.

1.21 CRYSTAL DIODES

A step forward was made when it was realized that active elements such as relays and vacuum tubes are not required to perform the operations essential in digital computers.¹ Any non-linear device has two states, one in which the impedance is high and one in which the impedance is low. Crystal diodes, for example, have two clearly defined states: one in which the impedance is about 200 ohms and one in which the impedance is greater than 50,000 ohms, and crystal diodes have the advantage that they can be driven from one state to the other by a one-volt signal. From the point of view of power dissipation, crystal diodes are far superior to vacuum tubes. The power dissipated in the 50,000 ohm state is negligible. In the 200 ohm state the power dissipated is only 5 milliwatts, while the equivalent vacuum tube diode dissipates one watt continuously in its heater. This lower power dissipation of the crystal, plus its mechanical simplicity makes it an ideal component for miniaturization.

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1. The University of Pennsylvania EDVAC and the Bureau of Standards SEAC are computers reflecting this principle.

Computers have been built in which all the logic (switching and arithmetic operations) is performed in crystal diode networks. Being passive elements, crystal diodes have a high degree of reliability, but because they are passive, the signal is attenuated as it progresses through a network of crystals. When the power level has fallen to where it can no longer operate other circuits, an amplifier is inserted to restore the signal to its original strength. A recent machine² used about twenty crystals for every tube. It has been found practical to drive as many as thirty-two crystals at a megacycle rate with one tube.

1.22 TRANSISTORS

A major forward step was made when it became possible to replace the tube amplifiers with small devices that dissipate less power. The transistor is such a device. It can be driven from one state to the other by a very low voltage. In addition, it works well with crystal diode circuits, since the transistor itself is a crystal device. Also, it is well suited to use in regenerative amplifiers. In an amplifier for use in a digital computer there is no premium on linearity; in fact, regeneration is desirable because it decreases rise time and increases the effective power gain. An all "semi-conductor" computer would represent an advance in the art and is to be attainable now. A transistor amplifier, described in a following part of this report, has been developed which will amplify half-microsecond pulses with rise times of less than 0.05 microsecond and which requires less than 50 milliwatts of power.

2. The Bureau of Standards SEAC

TYPICAL COMPUTATION SHEET

A	B	C	D	E	F	G
x	SIN A	\sqrt{B}	A & C	LOG D	COEF.	E x F
1.0					1	
1.05					4	
1.10					2	
1.15					4	
1.20					2	
1.25					4	
1.30					2	
1.35					4	
1.40					2	

FIG. 1-1

FIGURE 1-2 FOUR-ADDRESS CODE

FOUR-ADDRESS CODE

(OP, A1, A2, A3, A4)

OP = OPERATION TO BE PERFORMED

$\left. \begin{matrix} A1 \\ A2 \end{matrix} \right\}$ = ADDRESSES OF NUMBERS TO BE OPERATED ON

A3 = ADDRESS AT WHICH RESULT IS TO BE STORED

A4 = ADDRESS AT WHICH CODE GROUP FOR NEXT STEP WILL BE FOUND

FIGURE 1-3 NUMBER AS A POLYNOMIAL

$$a_n x^n + a_{n-1} x^{n-1} + \dots + a_1 x^1 + a_0 x^0 + a_{-1} x^{-1} + a_{-2} x^{-2} + \dots$$

WRITE IN POSITIONAL NOTATION

AS:

$$a_n a_{n-1} \dots a_1 a_0 . a_{-1} a_{-2} \dots$$

EXAMPLE: RADIX 10

$$77 = 3.1415$$

$$a_2 = a_1 = 0 \quad a_0 = 3 \quad a_{-1} = 1 \quad a_{-2} = 4 \dots$$

FIGURE 1-4 EXAMPLE OF RADIX SEVEN

7^3	7^2	7^1	7^0	7^{-1}	7^{-2}
343	49	7	0		

DECIMAL 1000 IN SEPTENARY CODE

2	6	2	6	
COUNTING				
2	6	2	6	= 1000
2	6	3	0	= 1001
2	6	3	1	= 1002
2	6	3	2	= 1003

2	6	6	6	= 1028
3	0	0	0	= 1029

CATALOG OF BLOCK DIAGRAMS

2.1 INTRODUCTION

Starting from schematics for certain basic logic elements this memorandum presents a fairly complete catalog of diagrams of the units required in a digital computer. The designs have the common feature of performing all logic without the use of active elements. Active elements are employed only as gain producing devices (repeaters) to make up for attenuated signals. Thus the designs can be implemented with vacuum tubes, transistors, magnetic amplifiers, thermistors, or any other devices that have gain at the frequencies requiring amplification.

Serial operation has been used in all the designs. In serial operation all the digits of a word or number are transmitted in series along a single wire with the least significant digit first. The interval between the rise of successive digit pulses is referred to as one digit time. The interval between successive numbers or words is commonly referred to as the word time. Digit times of one microsecond have proved to be very practical and words as long as fifty binary digits have been employed (equivalent to 15 decimal digits).

Transistors make excellent amplifiers for pulses occurring at a megacycle rate and the reader can equate one digit time to one microsecond whenever he wants an estimate of the computing times required by the various machines described.

The reasons for choosing serial operation instead of parallel are quite simple. In a parallel system, each digit of a number appears in a different circuit. In a parallel adder a separate adder stage is used for each digit, whereas in a serial adder only one adder stage is used, and this one stage handles all the digits. Not only are the arithmetic operations performed with fewer components in the serial machine, but switching is also simplified. To switch an n -digit parallel number requires n switches to switch the separate wires, whereas in the serial machine only one switch is required.

All of the digital computers that have thus far been put into operation have exhibited the common defects of undesirably high failure rate and very large size. These particular defects are easier to avoid in a serial design than in parallel machines, because a serial machine uses many less components.

2.2 BASIC BUILDING BLOCKS

The proposed computer elements are based on an assembly of a relatively small number of different kinds of basic units. The basic units have been limited to an or-circuit, an and-circuit, an inhibitor-circuit, an amplifier, and a storage cell based on a delay line. The designs suggested are similar to those in the EDVAC designed at the University of Pennsylvania and the SEAC designed at the Bureau of Standards. Some of the basic components have been described in the literature.* They are described again in the following paragraphs to provide a specific basis for the estimates of numbers of parts that are a goal of this study.

2.21 Or-Circuit

An n-terminal or-circuit (see Figure 2-1) develops an output when any one of its input terminals is energized. Crystal diodes are put in series with each input to prevent a pulse at one input from feeding back to any of the other inputs. An n-terminal circuit, therefore, requires n crystal diodes.

2.22 And-Circuit

An and-circuit having n input terminals develops an output only when all n of the input terminals are energized. In figure 2-2 each of the inputs is returned to a negative voltage and the output is clamped slightly below ground by X_{n+1} . Only when all of the inputs rise above

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*D. R. Brown and H. Rochester, "Rectifier Networks for Multiposition Switching", Proceedings of the I.R.E., Feb. 1949; and Tung Chang Chen, "Diode Coincidence and Mixing Circuits in Digital Computation", Proceedings of the I.R.E., May 1950.

ground will X_{n+1} be cut off, permitting the output to rise. Thus the output consists of the overlapping part of the inputs. An n -terminal circuit is seen to require $n + 1$ crystals.

Two terminal and-circuits are used extensively in serial computers for retiming signals. One terminal of the circuit is fed by the signal to be retimed while the other is fed by digit pulses from a master clock. There will be an output from the circuit only for the overlap of the master digit pulse and input signal. The circuit whereby the output is made a replica of the pulse from the clock is discussed in paragraph 2.24.

2.23 Inhibitor Circuit

An inhibitor terminal can be added to any and-circuit or or-circuit. Such a circuit operates as though there were no inhibitor terminal when the inhibiting pulse is not transmitted. When the inhibiting pulse is present, however, the circuit prevents any output from being developed. The inhibiting circuits used in the designs proposed herein are of the simple variety shown in Figure 2-3 where positive inputs synchronized in time are required. Note that the signal to be inhibited is passed through an eighth-digit delay line, while the inhibiting pulse is passed both through and around a quarter-digit delay line. This insures that the inhibitor pulse will, in effect, arrive earlier than the signal pulse and last longer. In the absence of input pulses, crystal X_4 will clamp the output at ground because input B is returned to a negative potential. Note that X_1 and X_2 are returned through the transformer to a positive potential. If input B goes positive (without an inhibiting pulse appearing on input A) X_4 will be cut off and the output voltage will rise until it is clamped at the positive potential to which X_1 and X_2 are returned. If there is an inhibiting pulse (positive) it is inverted by the transformer and will carry the cathodes of X_1 and X_2 negative, which will keep X_4 conducting, no matter what happens at B. Thus, if pulses A and B were written as a two-digit binary number AB, the circuit translates 01 into a 1 at the output. It translates 00, 10, and 11 into zero at the output.

2.24 Active Elements

Active elements will be used not as flip-flops or switches but as repeating amplifiers to make up for attenuation in crystal circuits and delay lines. The standard use will include a retiming feature as well as amplification. This is shown in Figure 2-4.

In the design of the machine, wherever a pulse is likely to suffer intolerable attenuation, deformation, or a variable delay, a circuit like that of 2-4 is inserted.

The assembly shown has two inputs, A and B. Input A is the pulse to be retimed and amplified. Input B comes from the master clock. This component supplies reference pulses (known as digit pulses) every digit time. These pulses are available in various phases, that is with various but accurately controlled delays of a fraction of a digit time. The pulse fed to B is selected to rise sometime between the expected rises and falls of the pulses on A.

If there is no input on A, there will be no output from the amplifier because of the and-circuit. If there is an input on A, when the digit pulse arrives the amplifier output will rise with a rise time determined by the digit pulse (assuming that the amplifier pass-band does not limit it). Part of the amplifier output is fed back through an or-circuit to the and-circuit. This insures that the output pulse will not fall until the reference digit pulse does, even though pulse A may have ended after B rose.

This reshaping with crystal circuits and an amplifier is the way in which every pulse is maintained with the desired time synchronization. Pulse A may vary somewhat in the delay it has suffered but the output pulse will still leave the amplifier at a time determined only by the reference pulse from the master clock. Thus, the pulses in the computer are made to have fixed durations and to occur at designated times.

In the tabulations of components in the following paragraphs an active element is intended to represent as one unit the tube, or transistor, with transformer. The term will include neither the and-circuit nor the or-circuit shown in Figure 2-4.

2.25 Storage Cell

The basic storage cell proposed is not a static device like a flip-flop but is an electric delay line plus an amplifier. When vacuum tubes are used, this type of storage saves one active element in a one-digit storage cell and is believed to be a more reliable use of active elements. In larger storage units more elements will be saved.

A block diagram of a cell is shown in Figure 2-5. The unit has three inputs: digit pulses, the signal to be stored, and an erase pulse. The digit pulses are received from the master clock every digit time and are used to retime (as discussed in paragraph 2-4) the output of the delay line before it is amplified and recirculated. The erase signal is received whenever new data are to be stored. It serves to erase the data in storage, blocking the delay line output from its input until the new data have been inserted.

The delay line may be long enough to store one word or just one digit of data. It is believed that up to fifteen-digit delay lines with lumped impedances can be built to hold the delay constant to within a small fraction of one digit time. Depending on the length of a word, it may be necessary to break one-word lines into sections and insert an amplifier between sections to retime and regenerate the pulses stored. To insure conservative estimates, the estimates made in following sections are on the basis of regeneration after every eight digits of delay.

2.26 Summary of Components Required in Basic Units

The circuits which have been discussed use the components listed below. This table will be used frequently in estimating the parts required in the larger assemblies:

TABLE 1

<u>Unit</u>	<u>Crystals</u>	<u>Digits of Delay</u>	<u>Active Elements</u>
N-Term'l Or-Circuit	N	0	0
N-Term'l And-Circuit	N+1	0	0
Inhibitor-Circuit	4	3/8	0
N-digit Storage Cell	10*	N	1*

2.3 SWITCHES

The switches are planned to combine a switching and a storage function. When a switch is given instructions to go to the k'th position, it goes there and it remembers that it is to remain there (self-locking operation). All the elements of the switches have been discussed in paragraph 2. How these elements are combined to make switches is described in the following:

2.31 Double-Throw Switches

A single-pole double-throw switch as shown in Figure 4-6 consists of a storage cell and a switch unit. When a "one" is stored in the storage unit, as the result of a pulse on the switching instruction lead, the left-hand and-circuit of the switch unit will pass signal "a" while the inhibitor blocks signal "b". When a zero is stored, the and-circuit will block signal "a" and the inhibitor-circuit in the switch unit will pass signal "b".

Whenever the switch is to be reset, an erase signal is fed to the storage unit, which then drops its old instruction and goes to position "b" unless the new instruction sets it to "a".

 * 1 active element will be used for $N \leq 8$ for $N > 8$, the number of active elements planned is the smallest integer $\geq \frac{N}{8}$. Six additional crystal diodes will be required with each active element.

The switch unit itself uses thirteen crystals $3/8$ digit of delay, and one active element, as can be ascertained from Figure 2.6 and table 1. A complete single-pole double-throw switch has 23 crystals, $1-3/4$ digits of delay, and two active elements. A two-pole double-throw switch would have two switch units and one storage unit. A three- or four-pole switch would have three or four switch units, one storage unit, and perhaps an extra amplifier to prevent the switch units from loading down the storage unit excessively.

2.32 Multiposition Switches

Switches with more than two positions can be assembled in a slightly different manner from the double-throw switches. Suppose, for discussion, that an eight-position switch is needed. A three-digit code must be sent to the switch to specify the position it is to select. A convenient way to operate such a switch is to translate the three-digit code into a six-wire code so that each digit is represented by signals of opposite phase on a pair of wires. In this system, a one is represented by a positive pulse on the positive bus and a negative pulse on the negative bus. A zero is represented by a negative pulse on the positive bus and a positive pulse on the negative bus. A three-terminal and-circuit is provided for each of the eight lines that may be selected. The and-circuits are operated by positive pulses, and all are connected to either one or another of each pair of wires representing the three digits of the position code. The and-circuit on the fifth (101) wire, for example, is connected to the positive bus of the pair representing the coefficient of 2^2 , to the negative bus of 2^1 and the positive bus of 2^0 . The three leads of the and-circuit will be energized by positive buses only when 101 is sent to the switch as instructions.

A single-pole eight-position switch is shown in Figure 2-7. The eight three-terminal and-circuits (one for each horizontal lead), plus the nine-terminal or-circuit make an easily studied crystal matrix which feeds another and-circuit for retiming of pulses and an amplifier on the output. The and-circuits are fed by switches S_0 , S_1 , and S_2 , which are driven by the switching instructions. These three switches are like the one shown in Figure 4.6. S_0 is

operated by the coefficient of 2^0 , S_1 by the coefficient of 2^1 , and S_2 by the coefficient of 2^2 . As the figure is drawn, only the and-circuit on line 7 (111) is energized. A pulse will be received at the output whenever a pulse is put on line 7. Pulses can be put on any of the other lines without getting to the output, because every other line is held negative by at least one lead from S_0 , S_1 , or S_2 . If an erase signal were sent to the three storage cells of S_0 , S_1 , and S_2 , the number 111 would be erased leaving 000, and the switches would be free to move to new positions and select another one of the eight inputs.

Based on this type of mechanization, an r -position switch requires n single-pole double-throw switches, where n is the smallest integer equal to or greater than $\log_2 r$. The switch requires $r(n + 1)$ crystals plus four crystals for retiming the output, and an output amplifier.

2.33 Summary of Components Required for Switches

The table below gives estimates of the crystals, digits of delay, and active elements required in switches of different degrees of complexity.

TABLE 2

<u>Type of Switch</u>	<u>Crystals</u>	<u>Digits of Delay</u>	<u>Active Elements</u>
1P.2T	23	1-3/4	2
2P.2T	36	1-3/4	3
4P.2T	63	6-1/2	6
1P.4T	61	2-3/4	4
1P.8T	105	6	7
1P.16T	160	7	9
1P.32T	311	8-3/4	11

where, 2P.2T = two-pole, two-throw switch.

2.4 ARITHMETIC UNITS

The following discussions show how the basic units discussed earlier are combined to perform the necessary arithmetic operations. The discussion of arithmetic units is preceded by some information on the handling of negative numbers.

2.41 Handling of Negative Numbers

The last digit place of every number is reserved to indicate the sign of the number. Positive numbers have a zero in the last place. A negative number is obtained by taking the two's complement of the positive number. This results in every negative number having a one in its last place.

A point of interest is that even though either or both the multiplicand and multiplier are negative the correct sign will be obtained for a product provided the negative numbers are increased from their normal length W to $2W-1$ by filling in ones before multiplying. This is necessary because the product of two W -digit numbers, where the last digit specifies sign, is a number $2W-1$ digits long. Unless the multiplicand and multiplier are increased to length $2W-1$ (when negative) the $2W-1$ place may be incorrect. This lengthening is not required for positive numbers, because the digits from W to $2W-1$ would be zeroes if they were filled in and would contribute nothing to the product.

A consequence of the above is that the product XY can be obtained to $2W-1$ places with $W(W-1)$ elementary additions provided X and Y are positive while $W(2W-1)$ additions will be required if both are negative. Where fast multiplication is desired it may be advisable to convert negative numbers to positive ones, multiply, and then adjust the sign of the product.

This system is equivalent to the ten's complement method used in decimal calculators. In a decimal calculator operating with three significant figures, a fourth place might be provided for the sign. The number -187 might be represented by its ten's complement 9813 . Then, for example, if -187 were required to be added to 500 the operation would be to add 9813 to 500 which gives 10313 and thus is recognized as 0313 since the machine was assumed to have only four digit places.

A negative number (two's complement) can be obtained in the binary computer by first forming the one's complement (changing all zeroes to ones and vice versa by means of an inhibitor circuit), and then adding one. Figure 2-8 shows several examples of binary arithmetic performed with negative numbers.

2.42 Adder

The adder can be considered as a translator with three inputs: addend, augend, and carry. It is a simple translator in that its output is a function only of the number of ones among its three inputs, as can be seen from the table below:

TABLE 3 - BINARY ADDITION

<u>INPUTS</u>			<u>OUTPUTS</u>	
<u>Addend</u>	<u>Augend</u>	<u>Carry</u>	<u>Sum</u>	<u>New Carry</u>
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
0	1	1	0	1
1	1	0	0	1
1	0	1	0	1
1	1	1	1	1

The combination 0 0 0 is automatically taken care of in the adder shown in figure 2-9. The three dashed circuits at the left of the block diagram recognize the other three situations among the three inputs. The situations are at least one "one", at least two "ones", and three "ones" among the inputs. If there is only one "one", it will go through the bottom or-circuit, the following inhibitor circuit, and then another or-circuit. After being reclocked and amplified it will provide a "one" as the sum. In this case none of the and-circuits on the A, B, and carry leads will have operated. If there are at least two "ones" on the A, B, and carry leads, at least one of the three two-terminal and-circuits in the dashed box will operate, with two results. The output of the three-terminal or-circuit at the bottom left of the diagram will be inhibited so that it makes no contribution to the sum. In addition, a carry signal will be developed which is delayed one digit, reclocked, and amplified to serve as the carry for the next

augend and addend. If there are three "ones", the three-terminal and-circuit at the top and left-hand side of the diagram will operate and develop a sum of one. The three two-terminal and-circuits on the left of the diagram will also have operated and provided the carry. Thus, the adder¹ table is mechanized with two active elements (amplifiers).

The inhibitor circuit in series with the carry lead should be noted. This circuit is fed by a word pulse as well as the carry digits. The word pulse is received in synchronism with the first digit of every number. The word pulse will inhibit the carry pulse if one is present and will prevent a carry developed in one problem from being used in the next. This feature is required in the addition of negative numbers.

The carry lead is brought outside the adder to facilitate subtraction. Suppose x is to be subtracted from y . The number y might be fed to the addend terminal and the number x fed through an inhibitor circuit to the augend terminal. The inhibitor would also be fed by digit pulses from the master clock, and the augend would therefore be the one's complement of x . A one would be inserted into the carry terminal in synchronism with the first digits of y and of the one's complement of x . The sum out of the adder would then be $x-y$ (see par. 4.1). The adder produces a sum within a fraction of a digit time after it receives an input. Thus there is only a small delay in obtaining the sum of two numbers.

Table 1 can be consulted to show that the adder of Figure 2-9 requires 38 crystals, $1\frac{3}{8}$ digits of delay, and two active elements.

2.43 Accumulator

A block diagram of an accumulator is shown in Figure 2-10. The output of the adder is fed back to its input through a w -digit delay line. The output of the delay line is continuously reclocked in the and-circuit in

¹ The operation of so many crystal circuits in series without amplifiers may be questioned but it is believed to be feasible at a microsecond rate. Experience may show, however, that another amplifier is required.

accord with digit pulses from the master clock. The timed pulses are then amplified in a one-stage amplifier to make up for attenuation in the delay line. Whenever a new accumulation is to be started, an erase signal is fed to the inhibiting circuit. This signal is w digits long and blocks the output of the delay line from the adder and insures that the new accumulation will start from zero. An accumulator to accumulate sums 48 digits long will require 76 crystals, 48 digits of delay, and 8 active elements.

2.44 Multiplier

The multiplier that is discussed in the following paragraphs is designed to multiply two positive members, each having W digits, in $W(W+1)$ digit times.¹ Operating at a megacycle rate, the product of two 48 binary digit numbers would be obtained in 2352 microseconds. It is believed most efficient to convert all negative members to positive ones before multiplying and to adjust the sign of the product according to the rules of algebraic multiplication (see paragraph 4.1). The components to be added to the multiplier to make the sign correction have not been included in this study. The multiplicand (x) is multiplied by the first (least significant) digit of the multiplier (y) in the first ($W+1$) period and by the W 'th digit of y during the w 'th ($W+1$) period. The w partial products are added together, with each partial product moved over one place with respect to the preceding one as it is accumulated.

The multiplication table in binary arithmetic is very simple. If it is desired to multiply the binary number x by a single binary digit, m , x is connected to the input of a switch that is held open if $m = 0$, and closed if $m = 1$. The output of the switch will be mx . Thus, in multiplying x by the successive digits of the number y , it is only required to recirculate x through a switch that is opened and closed at the appropriate times according to whether the successive digits of y are zeroes or ones.

Part of the multiplier is shown in Figure 2-11. The multiplicand (x) is stored in delay line 1, and the multiplier (y) is stored in delay line 2. After the first word period, $Sl-A$ and $Sl-B$ are thrown to position "b" and

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¹ This multiplier would obtain the correct sign for multiplication by negative members $W/2$ digits long.

the multiplier and multiplicand recirculate in their delay lines until the multiplication is finished. DL1 (delay line 1) storing the multiplicand has one more digit of delay than line DL2 in which the multiplier is stored. Therefore, after the first circulation of x through DL1, the least significant digit of x leaves DL1 just as the second least significant digit of y leaves DL2. After the $W-1$ 'th circulation of x , its least significant digit leaves DL1 just as the most significant digit of y leaves DL2.

The output of DL2 is fed continuously to an and-circuit. Every $W+1$ digits, an examining pulse is fed to the and-circuit, and if the digit of y coming out of DL2 is a one at that time, the and-circuit develops a one in its output. If, when the "examining" pulse comes along, the coefficient of y leaving DL2 is a zero, the and-circuit will have no output. Because DL2 has a delay of w digits, the inhibitor circuit in effect filters out the successive digits of y , choosing a new digit every $w+1$ digits times. The examining pulse is also sent to S2, where it is the erase signal of the storage cell associated with S2 (see paragraph 3.1). The output of the and-circuit goes to S2 as switching instruction and is stored there. Thus, S2 stores either a one or a zero, according to whether the digit of y examined is a one or a zero. The switch is arranged so that when a one is stored, S2 is closed, and when a zero is stored, it is open.

A new partial product is obtained at the output of S2 every $w+1$ digit times by the process described above. To accumulate them, an adder can be provided which accepts as one input the output of S2, and as the other input its own sum output delayed by w digits. The one digit place difference in the arrival of the two inputs of the adder automatically provides the "shift" feature necessary in adding the partial products. The only difficulty is that the product of two w -digit numbers may be a number $2w$ digits long which cannot be stored in the one-word delay line between the output of the adder and its input. Therefore, it is necessary to provide two delay lines and to use one of them to accumulate half the answer and the other for the second half.

As the complete block diagram (Figure 2-12) shows, at any time either DL4 or DL5 is receiving its input from the adder and feeding its output back into the adder. The

other delay line, at the same time, is feeding its own output into its input. Switching of the delay line is performed by the four ganged sections of S4. The switch is operated in such a way that the adder is connected to DL4 all of the first word period and to DL5 for one digit time longer of each succeeding word period, with the result that during the $W+1$ 'th word time the adder is connected to DL5 for the complete word period.

The switching instructions for S4 are developed in the following manner. The storage unit associated with S4 receives the word pulse from the clock every w digit times and uses it as an erase signal to empty its one-digit delay line. Every $w+1$ digit times the "examining" pulse is fed to the storage unit of S4 and stored there. S4 is arranged so that with a one in its storage unit, it selects position "a", and with a zero in its storage unit, it selects "b". Thus, S4 is at "a" from pulse 1 to pulse w , when the word signal at w erases the one in the storage unit. The switch goes to "b" and stops there for one digit time, then the $w+1$ pulse is written into the storage unit of S4 and the switch goes once more to "a". The second word pulse at $2w$ again erases the one in the storage unit and sends S4 to "b", where it stays for two digit periods until the second $w+1$ pulse at $2(w+1)$ writes in another one and pulls S4 to "a". Thus, S4 is held at "b" for one digit time longer each word period.

Figure 2-13 gives a digit-by-digit account of the operation of a four digit multiplier in multiplying 1001 by 1101. In studying the figure it is recommended that the reader keep in mind the position of S4 at each step so that he can tell where DL4 and DL5 are connected. It should also be noted that the outputs of DL4 and DL5 are always their inputs of four digits earlier.

A multiplier based on Figure 2-12 can be mechanized for 15 digit words with 204 crystals, $5w^1$ digits of delay, and 20 active elements.²

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1. The digits of delay required in inhibitors and switch memory units have not been counted. These uncounted delays might total eight or so digits.
 2. A multiplier for longer words would have longer delay lines and consequently would require additional retiming circuits. It is estimated that a 48 digit multiplier could be built with 324 crystals, $5w$ digits of delay, and 40 active elements.

2.45 Divider

The divider operates with repeated subtractions and shift operations much as one would do in pencil and paper division. Figure 2-14 shows two division examples. In the first one, three is divided by eight. First, it is seen that 1000 will not go into 11, so the first zero is written in the quotient. 100.0 will not go into 11, so the second zero is written. 10.00 will go into 11.0, so a one is written in the quotient and 10.00 is subtracted from 11.00. The remainder is 1.00. The binary point is again shifted in the divisor, giving 1.000 which goes exactly once, and another one is written in the quotient giving an answer of 0.011 or $0 \times 1/2 + 1 \times 1/4 + 1 \times 1/8$ equal to $3/8$.

It should be noted that at each step the divisor is either subtracted from the remainder or nothing is subtracted and that a shift to the right is made each time before the divisor is subtracted. In effect, the successive subtrahends are obtained by repeated divisions of the divisor by two. For machine operation, the awkward part of the above process is that it cannot be ascertained whether a subtraction should be made without making it and seeing whether or not the remainder is positive or negative. If the remainder is negative, the subtrahend should be added back. This necessity for sometimes adding back the subtrahend may be avoided. Let x be the subtrahend and R the minuend. Suppose x is subtracted from R and the remainder found to be negative. During the next step the machine should subtract $x/2$ from R , but the machine has lost R by subtracting x from it. R can be regained and $x/2$ subtracted at the same time by adding the factor $x/2$ to the negative remainder $R - x$ which gives the desired result $R - x/2$. Thus, on the successive steps the machine either subtracts half the previous subtrahend or adds half the previous subtrahend, depending on whether the previous remainder was positive or negative. The process is further simplified by avoiding subtraction through adding the two's complement of the subtrahend rather than subtracting the subtrahend.

An example of the simplified division process is shown in Figure 2-14. The machine is assumed to have five digit places. The first step is to fill out the divisor and dividend to $2w-1$ places, and then to form the complement of the divisor (according to the methods discussed in par. 4.1).

The divisor complement is first added to the dividend. The $2w-1$ 'th digit of the sum is noted. In the example, the digit is a one, indicating a negative result. The machine then writes a zero in the quotient, drops out the $2w-1$ 'th digit of the previous sum, and adds half the divisor (divisor shifted one place to the right). The $2w-1$ 'th digit is again examined and is found to be a one. Another zero is written in the quotient, the $2w-1$ 'th digit is dropped out, and the divisor is again shifted and added. This time the $2w-1$ 'th digit is zero, indicating a positive sum. A one is written in the quotient, and the complement of the divisor is shifted and added. This process is continued until the five-digit answer 0.0110 is obtained. Note that the first operation was made with the binary points of the divisor and dividend lined up. In general, it would be necessary to start with the least significant digit of the divisor written under the most significant digit of the dividend. $2w(2w-1)$ digit times are required for division in a general purpose machine.

The divider block diagram is shown in Figure 2.16. The divisor is stored in delay line 1 and recirculates there becoming available every $2w-1$ digit times. The one's complement of the divisor is taken by the inhibitor circuit fed by DL1 (delay line 1). Every $2w-1$ digit times switch S2 selects either the one's complement of the divisor or the divisor itself to go into the adder. The switch selects the one's complement when it is desired to subtract. However, to obtain subtraction it is necessary to add the two's complement. This is done by bringing out the carry terminal of the adder, and whenever S2 is thrown to select the one's complement a one is sent into the carry terminal and, in effect, makes the augend the two's complement.

The storage cell of Switch S2 receives an erase signal every $2w-1$ digit times. At the same time, the switch receives a one or a zero from the inhibitor circuit on the adder output. If this inhibitor sends a one to the switch, the $2w-1$ 'th digit of the sum just completed was positive and switch S2 goes to position "b" to select the one's complement of the divisor for the next addition. The output of the inhibitor circuit is also sent to the carry terminal of the adder, so that when S2 is at "b", a one will be injected to convert the one's complement to a two's complement. Each output of the inhibitor is also a digit of the quotient, for if the $2w-1$ 'th digit of the sum is a zero, a one should be written in the quotient and the inhibitor supplies that one.

It is written in delay line 3, which has a circulation time of $2w$. Since a new quotient digit is received every $2w-1$ 'th digit time, delay line 3 has as its output the digits of the quotient in reverse order to that in which they are obtained, which puts the least significant digits first as they should be.

The above discussion shows how the augend is obtained for the adder. The addend is obtained from S1B. This switch selects the dividend during the first $2w-1$ period, and thereafter selects the previous sum from delay line 2. Note that an inhibitor circuit between the adder and DL2 blocks out the $2w-1$ 'th digit each time to keep the remainder from growing longer than $2w-1$. Since delay line 2 has $2w$ delay and delay line 1 has $2w-1$ delay, the augend arrives 1 digit early each $2w-1$ period with respect to the addend. This feature supplies the successive divisions by 2 that are required.

Delay line 4 exists merely to supply the $2w-1$ pulse that is sent to S2 and the inhibitor circuit on the adder output. Switch S1 is driven by the master clock. Its sections are switched to "a" at the end of the computation period to empty the lines of the dividend, divisor, and $2w-1$ pulse preparatory to solving a new problem. After $2w-1$ digit times, all sections of S1 are thrown to "b" and recirculate their data.

An estimate based on Tables 1 and 2 of the parts required by the divider of Figure 2-16 shows that to handle 48 digit numbers, 371 crystals, 384 digits of delay, and 51 active elements would be required. This assumes that the delay lines have their data regenerated every $w/2$ digits. If the data are regenerated only every w digits, only 36 active elements are required. The divider is seen to be of about the same complexity of the multiplier.

2.46 Square Rooter

This machine obtains the square root of a number to w places in $2w^2$ digit times. It mechanizes the ordinary arithmetic method of taking square roots. Before describing this unit, it is well to consider the algebraic basis of the arithmetic method normally used.

2.461 Development of Operating Principle

In Figure 2-17 an arithmetic problem is solved in the right-hand column, and the justification for each step is shown in the left. Note that a new digit place is obtained in each step, and that the only processes involved, apart from adding zeroes, are multiplication by a number less than ten and subtraction. The method can be extended to binary operation as shown in Figure 2-18. Binary operation is somewhat simplified because the only processes needed besides adding zeroes are multiplication by one or zero and subtraction.

For machine operation, there is a drawback to the method illustrated in Figure 2-18. Sometimes, as in the fourth step, the subtrahend must be multiplied by zero, not one, before it is subtracted. The only way the machine can find out it should have multiplied by zero is for it to assume it should multiply by one, form the subtrahend on that assumption, and subtract it. If the machine obtains a negative remainder it knows that it should not have subtracted anything at all. The simplicities of binary arithmetic make it possible to devise a method of operation in which the necessity of adding back the subtrahend is avoided.¹

Suppose, with reference to the algebra of Figure 2-17, that the machine is taking the square root of x and has just established the partial answer

$$y_{n-1} = h_1 + h_2 - - - h_{n-1}$$

and is about to determine the value of h_n , where h_n will be either a one or a zero multiplied by 2^p where p is an integer.

At this stage the remainder in the machine is

$$R_{n-1} = x - y_{n-1}^2$$

¹

This procedure is believed to be a new contribution.

and the next operation will be to form the trial subtrahend

$$(2 y_{n-1} + 2^p) 2^p$$

and subtract it from R_{n-1} , which will leave as the new remainder

$$R_n = x - (y_{n-1} + 2^p)^2 = x - y_n^2$$

If R_n is a positive number the machine will enter a one as the coefficient of 2^p in the answer and proceed to obtain the coefficient of 2^{p-1} in a similar manner.

If, on the other hand, R_n turns out to be negative, the machine should write 0 as the coefficient of 2^p in the result (thus $y_n = y_{n-1}$) and subtract

$$(2 y_n + 2^{p-1}) 2^{p-1} = (2 y_{n-1} + 2^{p-1}) 2^{p-1}$$

from R_{n-1} , which would give the correct value

$$R_{n+1} = x - (y_n + 2^{p-1})^2 = x - (y_{n-1} + 2^{p-1})^2$$

Unfortunately, the machine does not have R_{n-1} available because it has subtracted and obtained R_n . However, to get the desired R_{n+1} , the machine need only add to the erroneous R_n .

$$[2 y_n + 3 (2^{p-1})] 2^{p-1}$$

instead of subtracting

$$(2 y_n + 2^{p-1}) 2^{p-1}$$

which would have been done if R_n had been positive. There is only a slight difference in the two operators above. When a positive remainder is obtained, the machine adds 01 times 2^{p-1} to $2y$ and then adds 2^{p-1} zeroes at the end of the sum to obtain the new operator. In the event that a negative remainder is obtained, the machine adds 11 (3) times 2^{p-1} to $2y$ and then adds 2^{p-1} zeroes at the end of the sum. On Figure 2-19 two examples are given of the simplified method.

The square root machine, Figure 2-21, obtains a new digit of a w -digit answer every $2w$ digit times. In each $2w$ period the machine either subtracts or adds, depending on whether the digit determined in the previous period is a one or a zero. The minuend or the addend for a given $2w$ period is obtained from the remainder or the sum of the previous period. The subtrahend or the augend is formed from the answer digits already obtained. The manner of forming the operator is dependent upon the value of the digit determined in the preceding step as is the decision to whether the operator is added or subtracted.

Before going into the discussion of the block diagram it is well to consider in detail how the square root of a specific number would be taken. For this purpose a relatively short number is more convenient than a larger one. In Figure 2-20 the second example of Figure 2.19 (for which $W = 5$) has been rearranged in the sequence in which the digits would be operated upon by the machine. The top row lists the time (measured in digit times from the start of the problem) at which the digits listed arrive. The second row lists the digits of the operators that are the digits that make up the operators used as subtrahends or augends. The fourth row shows the results of subtracting or adding the operators above, and the next row shows the answer digits as they are obtained. The final row shows when the answer digits are required to reappear in order to be used in the third row.

As Figure 2-20 shows, in the first period the first operator is the number (of $2w$ digits = 10) whose square root is desired, while the second operator is a one inserted at digit time $2w - 1$ (9). The last digit of the remainder is examined at time $2w$ (10). Since the digit examined is a zero, C_1 is written as one, the most significant digit of the answer. If the $2w$ 'th digit were one, zero should be written in the answer as the coefficient of $2w$; since in the example C_1 is written as one, the remainder of the first step is used as the minuend for the next period. The subtrahend is formed by the digit C_1 delayed $2w-1$ (9) digit times and by the one subtracted in period one delayed by $2w-2$ (8) so that it arrives at digit time 17. The digit C_1 was a one, so in the second period subtraction is performed and the $2w$ 'th digit of the remainder examined. This digit is seen to be a zero, so the remainder obtained on the second $2w$ period is used as the minuend for the third period and a one is written in the answer as C_2 .

The subtrahend for the third step is formed from the digit C_1 , delayed $2w-1$, the digit C_2 delayed by $2w-3$, and a one delayed $2w-2$ (8) from the time (17) it was used in step 2 to arrive at 25.

The remainder in the third step has a one in the $2w$ 'th place, indicating it is negative. The remainder is, therefore, used as the addend for the fourth $2w$ period and a zero is written as C_3 . The augend for the fourth period is formed by delaying the number $C_1 C_2$ by $2w-1$ digit times from the time it was used previously, by delaying digit C_3 $2w-5$ digits (so it arrives at time 35), and at digit times 33 and 34 writing ones. The one at time 33 is the one written at time 25 delayed by $2w-2$. The one written at time 34 is written because the remainder of the third period was negative.

From the figure it is seen that the sum in the fourth step is still negative. The sum is used as the addend for the fifth step and another zero is written in the answer as C_4 . The augend for the fifth step is formed by the word $C_1 C_2 C_3$ delayed by $2w-2$ from the time it was used in the

fourth step, the digit C_4 delayed by $2w-7$, so that it arrives at time 43 , and the word 11 delayed by $2w-2$ from the time it was used in the fourth period. When this augend is added, the $2w$ 'th digit of the sum is a zero, and a one is written in the answer as C_5 .

2.462 Rules of Operation for Square Root Machine

The procedure can be generalized into the following rules for using an adder to obtain the square root of x , where the square root is written as $C_1 C_2 C_3 C_4$ etc., and each coefficient is a one or a zero.

Rule 1 - Examine every $2w$ 'th digit of the output of the adder, and if the examined digit is zero, write one as the answer digit. If examined digit is one, write zero as answer digit.

Rule 2 - In the first $2w$ period, use x as the addend. In all other periods, use the output of the adder delayed by $2w$ digit times.

Rule 3 - In the first $2w$ period form the augend for the adder by taking the two's complement of a number that consists of a single one written at digit time $2w-1$. In all other periods determine the augend according to rule 4.

Rule 4 - If the answer digit C_{n-1} determined in the $n-1$ 'th $2w$ period is a one, form the augend for the n 'th period by rule 5. If C_{n-1} is a zero, form the augend by rule 6.

Rule 5 - Form the augend for the n 'th period by taking the two's complement of q where q consists of the three parts

- (a) The word $C_1 C_2 - - - C_{n-2}$ delayed by $2w-1$ from its use in the previous step.
- (b) The digit C_{n-1} delayed by $2w+3-2n$ from the time it was obtained in the previous step.
- (c) The digit one written two digits earlier than C_{n-1} .

Rule 6 - Form the augend for the n 'th period from the three parts listed below:

- (a) The same as in Rule 5.
- (b) The same as in Rule 5.
- (c) The same as in Rule 5, but with an extra one inserted at digit time $2w+2-2n$.

2.463 Block Diagram

One way of studying the block diagram (figure 2-20) is to take each of the rules stated in 4.62 and see how they are implemented.

Rule 1 - The machine receives a pulse every $2w$ digits from the master clock. This pulse goes to the inhibitor circuit that is connected to the output of the adder. The inhibitor, therefore, examines every $2w$ 'th digit of the adder output and develops a one if the adder digit is zero and develops a zero if the adder output is a one. Thus the output of the inhibitor can be taken as the successive digits of the square root of x . Each output of the inhibitor is stored temporarily in a one-digit storage cell until it can be written into $DL4$, which stores the complete answer.

The examining pulse that occurs every $2w$ digits also goes to the one-digit storage cell to act as the erase signal and remove C_{n-1} when C_n is stored.

Rule 2 - In the first $2w$ period, $S1$ is at position "a", and the addend for the adder is x transmitted through this position. Thereafter, $S1$ is at "b" and the addend is the adder output delayed by $2w$ digits in $DL1$.

Rule 3 - Coincidental with the transmission of the least significant digit of x into the machine, a start signal is received from the master clock. The start signal sets $S2$ to position "a". The start signal also progresses through $DL5$ and $DL2$ to arrive at an inhibitor circuit feeding $S2$ at time $2w-1$. The inhibitor circuit has as output, therefore, the one's complement of 0100 --- 0. To convert this to a two's complement, the start signal is fed directly to the carry terminal of the adder.

Rule 4 - The operating instructions for switch S2 are obtained from the inhibitor in the adder output as well as from the start signal. S2 is of the type discussed in 3.1. Every time a new digit of the answer is determined, it is fed to the input terminal of the storage cell associated with the switch and sets it to "a" if the digit is a one or to "b" if the digit is a zero. Coincidental with the answer digit, the $2w$ pulse is fed to the erase terminal of the switch storage cell to remove the previously stored instruction, so that the switch can move to the new position. Setting switch S2 to "a" is equivalent to saying, "Follow Rule 5" and setting switch S2 to "b" is equivalent to saying "Follow Rule 6".

Rule 5 - When digit C_1 is determined it goes into the one-digit delay line DL7 and recirculates there until C_2 is determined. At time $2w+1$ the start signal leaves DL6. It is inhibited, however, by the $2w$ pulse delayed one digit in DL3. The recirculated start signals from DL2 are all delayed two digits by DL6 and reappear at the output of DL6 once in each $2w$ period at the times listed below:

<u>Period</u>	<u>Time</u>	<u>Digit entered in DL4</u>
2	$2w+1$	none
3	$4w-1$	C_1
4	$6w-3$	C_2
5	$8w-5$	C_3
-	---	--

The output of DL6, in each case above except the first (when it is inhibited), goes to an and-circuit in the one-digit storage cell and lets a digit of the answer into DL4. The input of DL4 is also fed through an inhibitor to the "a" input of S2 and back to the adder to mechanize part "b" of Rule 5. Since C_1 first enters DL4 at $4w-1$ it will re-enter it at $6w-2$ just behind the first entry of C_2 , which is as it should be to fulfill part "a" of Rule 5.

Part "c" of Rule 5 is fulfilled by the recirculated start pulse from DL2. It may be noted that DL6 provides the two-digit delay required between C_{n-1} and the "one" digit of part "c" of Rule 5.

The inhibitor at terminal "a" of S1 will provide the one's complement of q (see Rule 5). The two's complement is obtained by feeding the output of the inhibitor on the adder output back into the carry terminal of the adder. The one-digit delay line (DL9) is required to get the carry at $2w+1$ rather than $2w$.

Rule 6 - Parts "a" and "b" of this rule are fulfilled by the connection of the input of DL4 into terminal "b" of S2. Part "c" is fulfilled by the connection of the output of DL2 into terminal "b" of S2 both directly and through the one-digit delay line DL8.

In all discussions above it has been assumed that x is a $2w$ digit number. This may not be the case in some computers. To convert x into a $2w$ number it may be delayed w digits, which adds w zeroes to it. The delay may be obtained through a tap in DL1. Another expedient would be to take x as a w -digit number and send the first $2w$ pulse at time w , the second at $3w$, etc.

The block diagram has been analyzed for its component requirements. It is believed that a square rooter to give 48 digit answers can be mechanized with 338 crystals, 312 digits of delay and 45 active elements. It may be noted that a square root machine is no more complex than a divider.

2.47 Summary of Components Required for Arithmetic Units

Two sets of estimates have been prepared. Table 3 lists the components required for units handling 15 binary digit numbers ($4\frac{1}{2}$ decimal place). Table 4 lists the components for 48 (14 decimal place) digit numbers. It should be noted that an adder would be the same in either case.

TABLE 3

COMPONENTS REQUIRED FOR 15 DIGIT ARITHMETIC UNITS

<u>UNIT</u>	<u>CRYSTAL DIODES</u>	<u>DIGITS OF DELAY</u>	<u>ACTIVE ELEMENTS</u>
Adder	38	2	2
Accumulator	52	15	4
Multiplier	204	85	20
Divider	179	128	19
Square Rooter	182	98	19

TABLE 4

COMPONENTS REQUIRED FOR 48 DIGIT ARITHMETIC UNITS

<u>UNIT</u>	<u>CRYSTAL DIODES</u>	<u>DIGITS OF DELAY</u>	<u>ACTIVE ELEMENTS</u>
Accumulator	76	48	8
Multiplier	324	85	40
Divider	371	384	51
Square Rooter	338	312	45

2.5 MISCELLANEOUS UNITS

In addition to the units discussed above, certain others are useful in a computer. Some are discussed below.

2.51 Translator

This unit translates one set of numbers or words into another set. Storage may be regarded as translation in which addresses are translated into the words stored at the addresses.

Translators are useful in developing switching orders. At the completion of some process, it may be necessary to develop a new set of orders. When the orders must be developed in a certain sequence, a binary counter can be used to develop the input for the translator. Whenever the next set of orders are required, a pulse is fed to the counter. The binary count number is used as the switching instruction for a switch. Every time the counter receives an input pulse the switch will be advanced one position and will put a pulse on the selected lead. The various output leads of the switch will be connected to a group of or-circuits. One or-circuit will be required for each digit of the translator output. Figure 2-22 shows a scheme for generating 8 sets of 3 digit words. To generate n digit words n or-circuits would be required. No more than 8 leads would be required for any or-circuit. The translator shown develops the output word in parallel. If the or-circuits are fed to taps in a delay line, the output word will be received serially from the output of the delay line. The or-circuits have the same function as the coil maze in the Laboratories' Mod 6 computer.

2.52 Binary Counter

Figure 2-23 shows how each stage of a binary counter can be made from a one-digit memory cell (see paragraph 2.5) plus an inhibitor and an and-circuit. In Fig. 2-23, if the count is at 01 and a one is sent into the counter, the one in the first stage will be admitted to the second stage. The one that was in the first stage inhibits the one input and the first stage therefore goes to 0 and the count is 10. If another one is sent into the counter, it will enter the first stage and the count will advance to 11. If another one is fed in, the first two stages will set to zero and the third will receive a one making the count 100. It is seen that each stage is a dynamic flip-flop. This type of counter can be used only to count synchronized input pulses but that is all that a counter is expected to do in a serial computer.

In a serial machine binary counters can often be replaced by simpler devices. Suppose that it is desired to time some operation and know when 64 digit times have elapsed.

A six-stage counter could be used or a digit pulse could be circulated in a seven and a nine digit delay line. If an and-circuit were fed by the two delay lines, 63 digit times would elapse before the and-circuit were operated. If the output were fed through a one digit delay line the desired 64 digit delay would be obtained.

2.53 Shift Registers

Shift registers are sometimes needed to take data at a low rate, from a magnetic drum for example, and re-transmit it at a rapid rate. A shift register that is loaded serially may be read out in parallel on w leads or in series on one lead. Each stage of such registers can be built around a one-digit memory cell. Fig. 2-24 shows two stages of each kind of register. The numbers in each cell are erased and advanced to the next cell whenever an advance pulse is received.

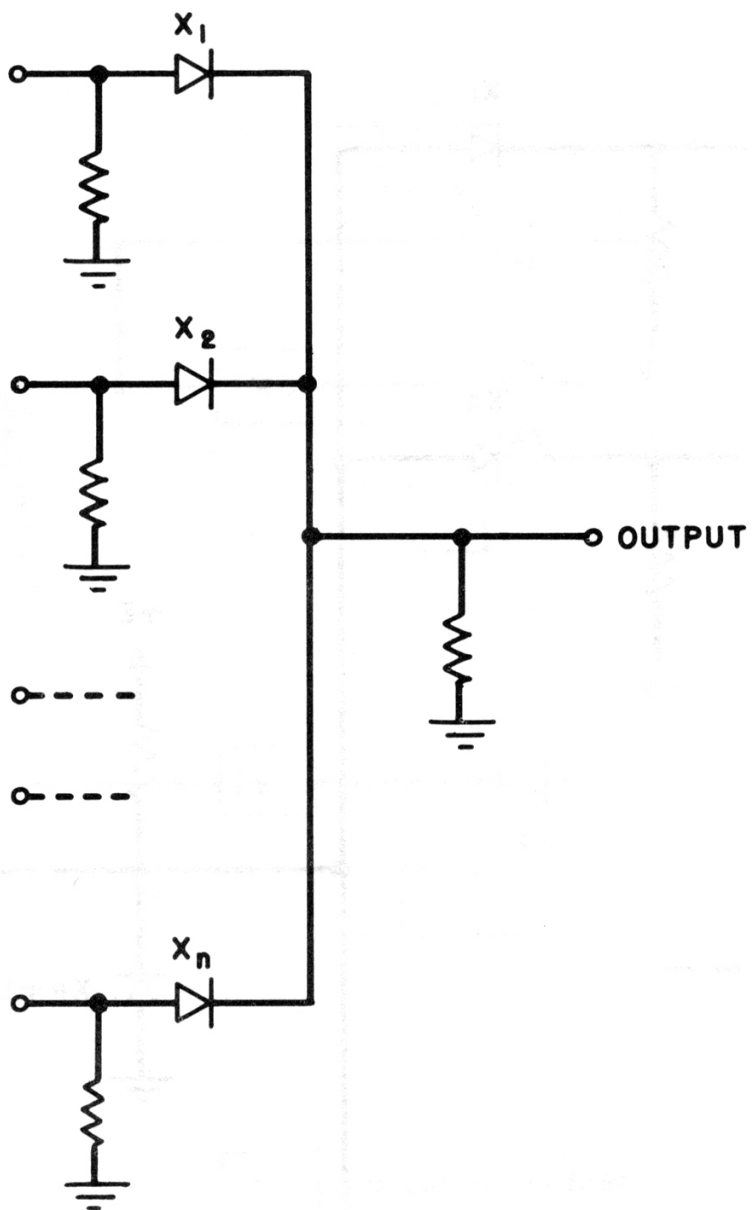
Advance pulses will be received every time a new digit is to be loaded. When a number is in the register, the advance pulses can be stopped and the number can be stored until it is required. In the case of the parallel-read-out registers, extra and-circuits are used at each stage. These are fed by the read-out signal.

Besides their use in changing the rate of transmission of data, the shift registers described above can store words for integral multiples of a digit time. Where the storage period is an integral multiple of a word time it is more efficient to use delay lines as discussed in paragraph 2.5. It may be mentioned that in a synchronous computer tapped delay lines can replace shift registers for the conversion of serial to parallel data and vice versa.

2.6 CONCLUSIONS

A catalog of computer units has been presented. The units make use of active elements only as repeating amplifiers. It is shown that multipliers, dividers, etc. can be built with less than 50 such amplifiers.

POSITIVE
INPUTS



SYMBOL

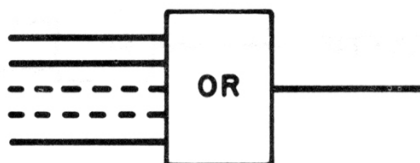


FIGURE 4-1
N-TERMINAL
OR-CIRCUIT

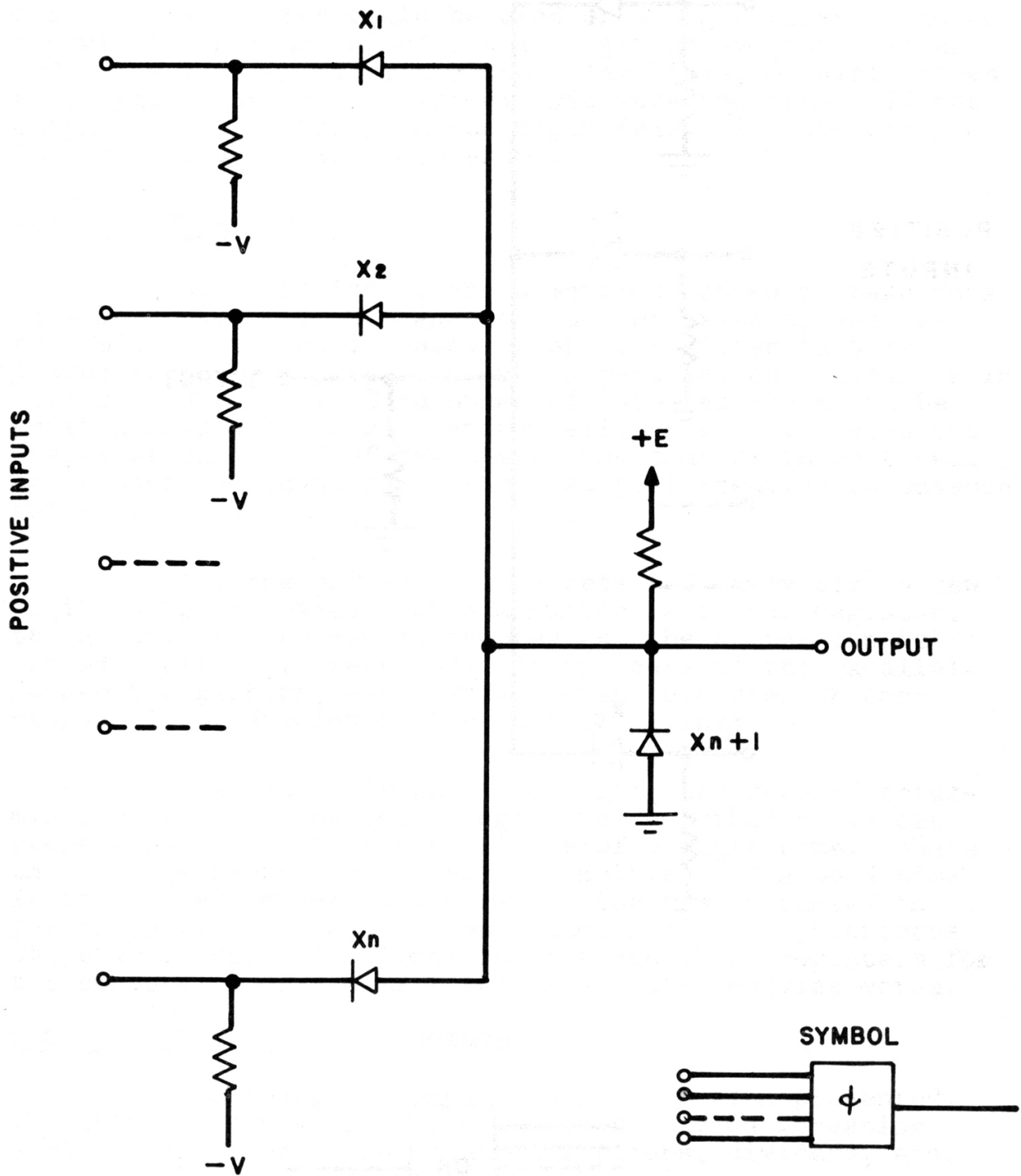
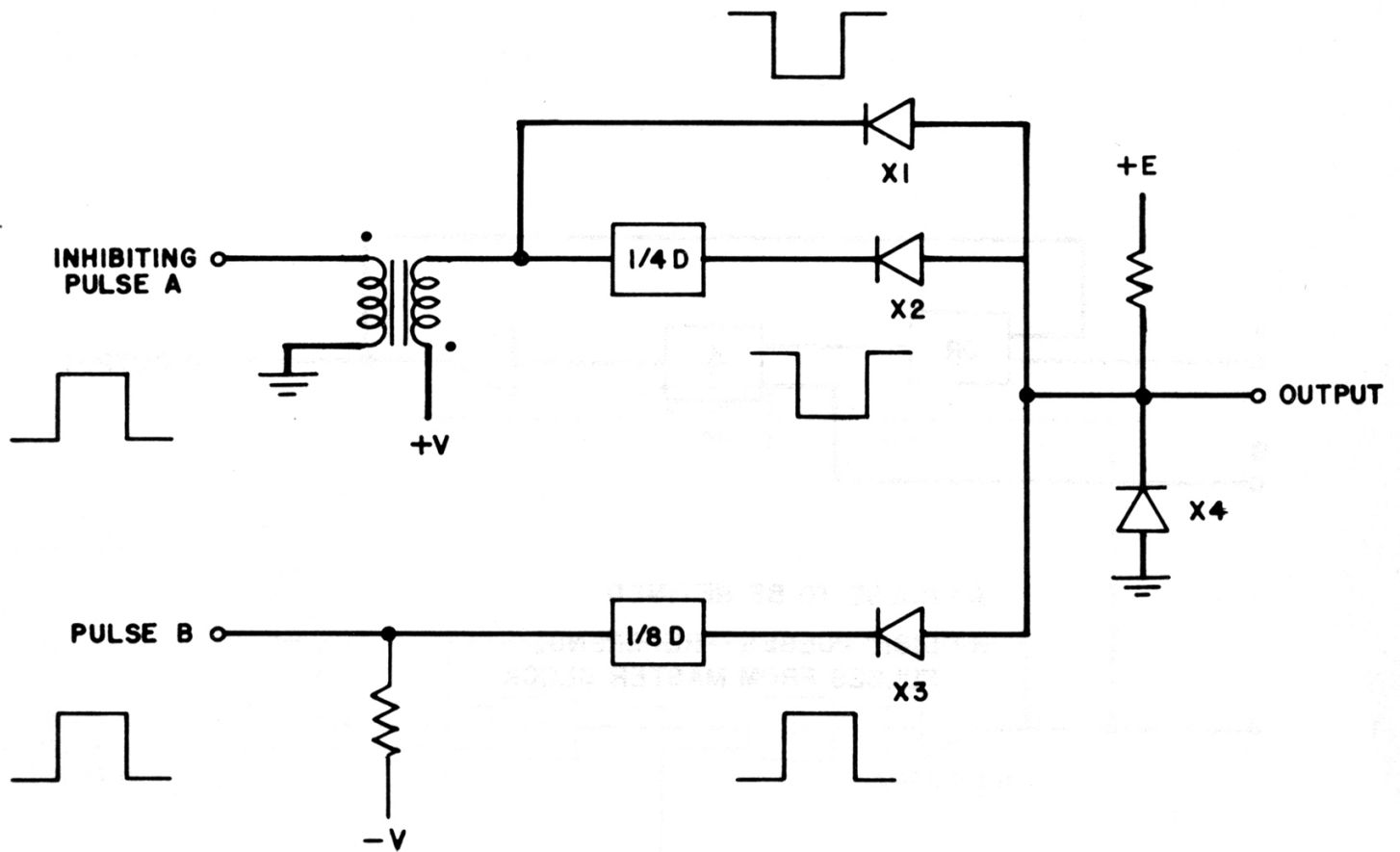


FIGURE 2-2
N - TERMINAL
AND - CIRCUIT



YD = DELAY OF Y - DIGITS

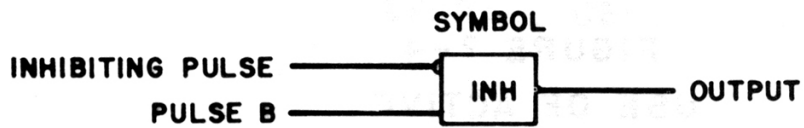
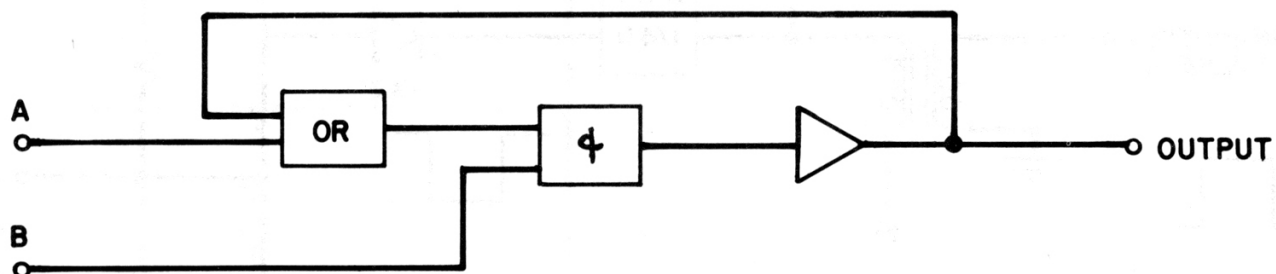


FIGURE 2 - 3
INHIBITOR
CIRCUIT



A = PULSE TO BE RETIMED

**B = DIGIT PULSES - REFERENCE
PULSES FROM MASTER CLOCK**

**FIGURE 2-4
USE OF ACTIVE
ELEMENTS**

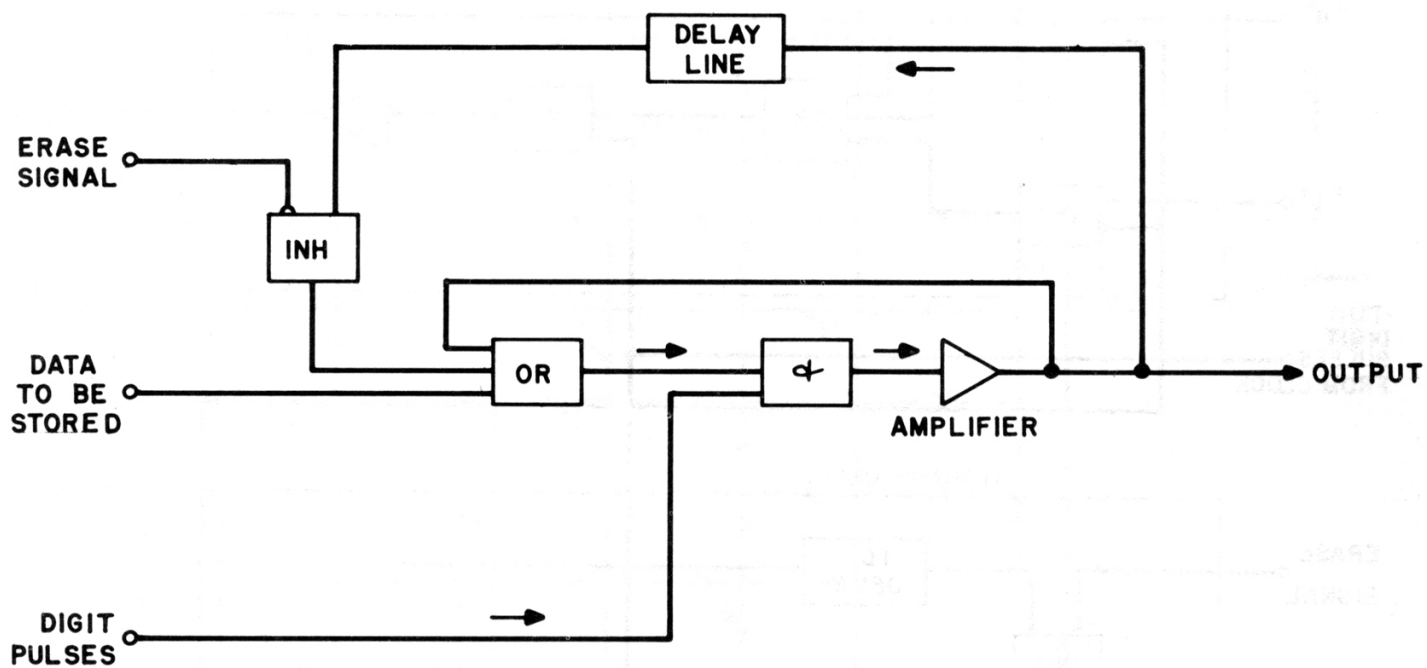
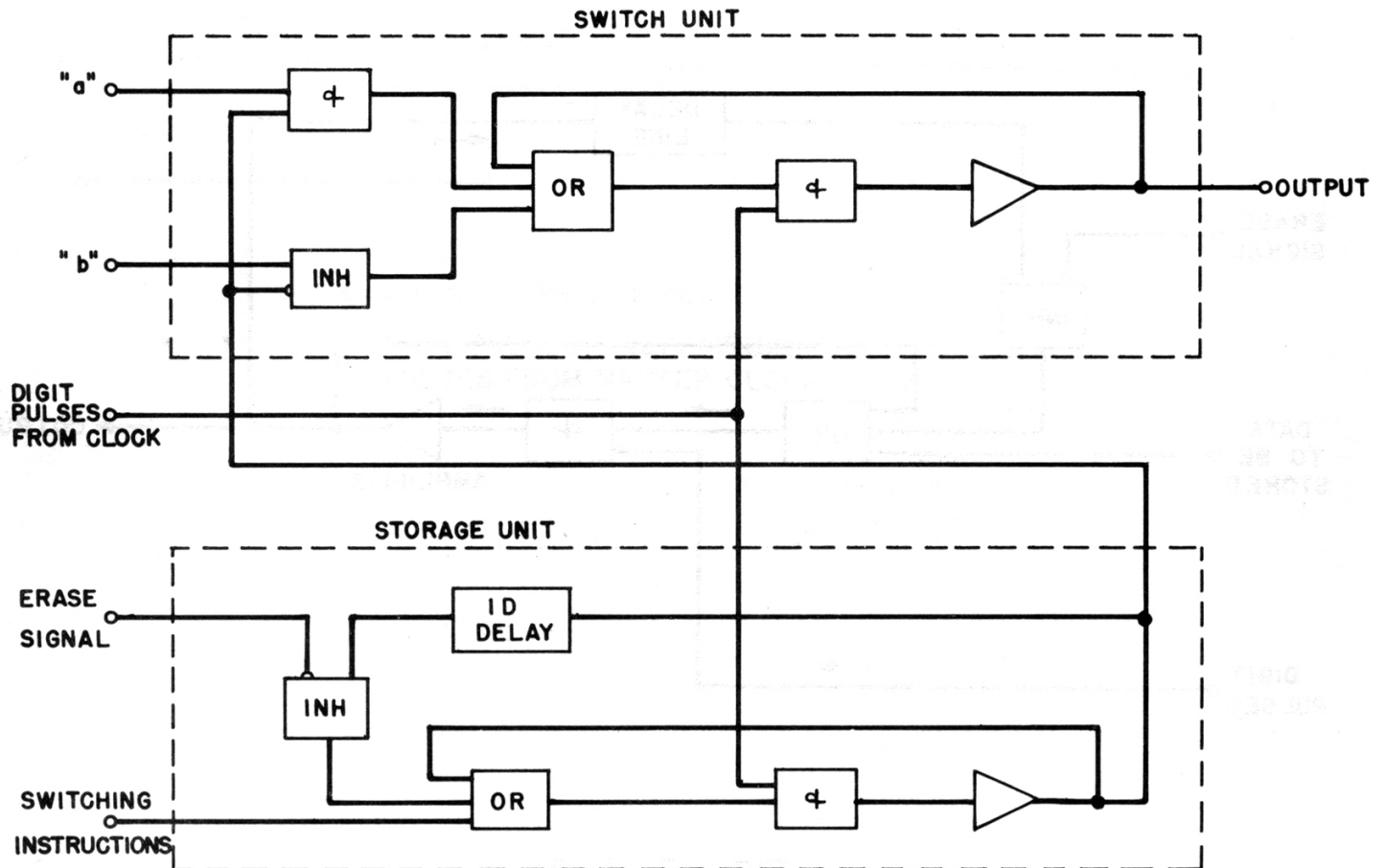
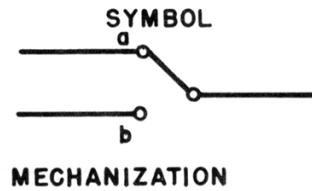
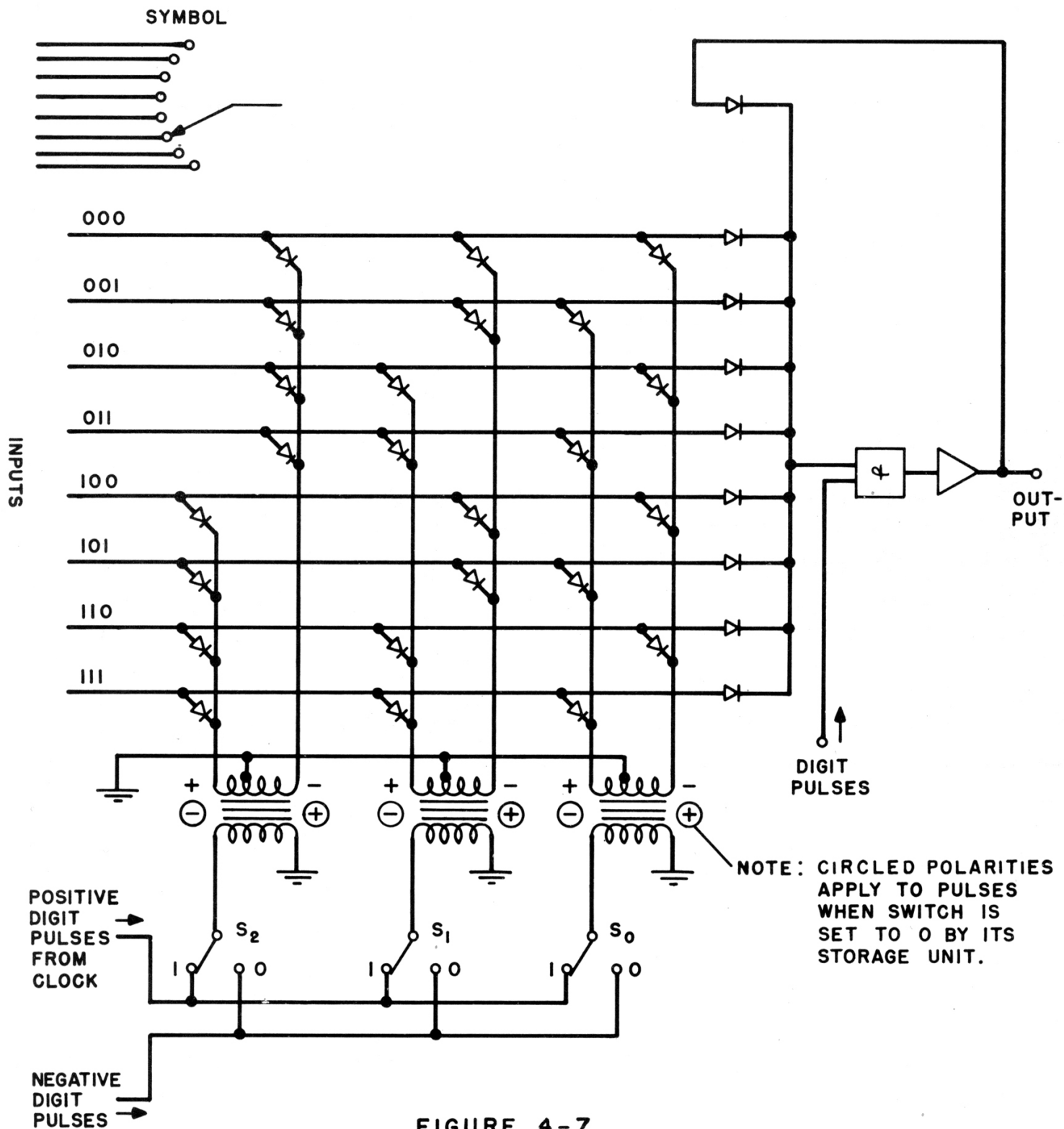


FIGURE 2-5
STORAGE CELL



0 SETS SWITCH TO "b"
1 SETS SWITCH TO "a"

FIGURE 2-6
SINGLE POLE
DOUBLE THROW
SWITCH



**FIGURE 4-7
SINGLE-POLE
EIGHT-POSITION
SWITCH**

NEGATIVE NUMBERS IN A 5 SIGNIFICANT
DIGIT SYSTEM WITH ONE IN SIXTH
PLACE SIGNIFYING THAT THE NUMBER
IS NEGATIVE

(A) FORMATION OF NEGATIVE NUMBERS

+8 = 001000
ONES
COMPLIMENT = 110111
ADD ONE
∴ -8 = 111000

CHECK -8 + 8 = 0
+8 = 001000
-8 = 111000
SUM = 1|000000 = ZERO
TO THE MACHINE

(B) ADDITION

-8 + 5 = -3
-8 = 111000
+5 = 000101
SUM = 111101 = -3
CHECK +3 = 000011
SUM = 1|000000 = ZERO

-8 + 15 = 7
-8 = 111000
+15 = 001111
SUM = 1|000111 = 7

(C) MULTIPLICATION

-8 X 7 = -56
-8 = 1000
7 = 111
1111000
0000111
1111000
1111000
1111000
0000000
0000000
0000000
0000000
1001000
↑ SHOWS ANS. IS NEG.

CHECK
-56 + 56 = 0
-56 = 1001000
+56 = 111000
1|0000000

(D) ANOTHER MULTIPLICATION

-8 X -7 = +56
-8 = 1111000
-7 = 1111001
1111000
0000000
0000000
0000000
1111000
1111000
1111000
1111000
0111000
↑ INDICATES POSITIVE NUMBER

FIGURE 2-8
HANDLING
NEGATIVE NUMBERS

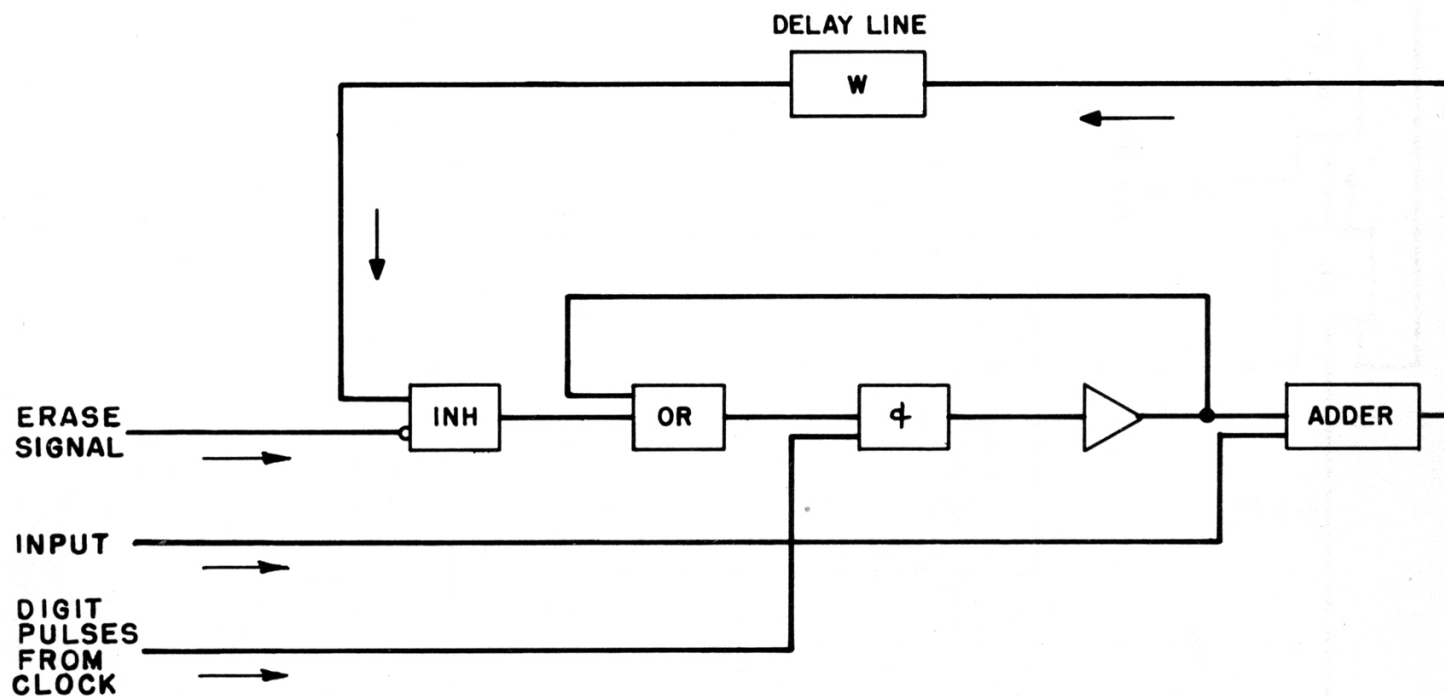


FIGURE 4 - 10
BLOCK DIAGRAM
OF
ACCUMULATOR

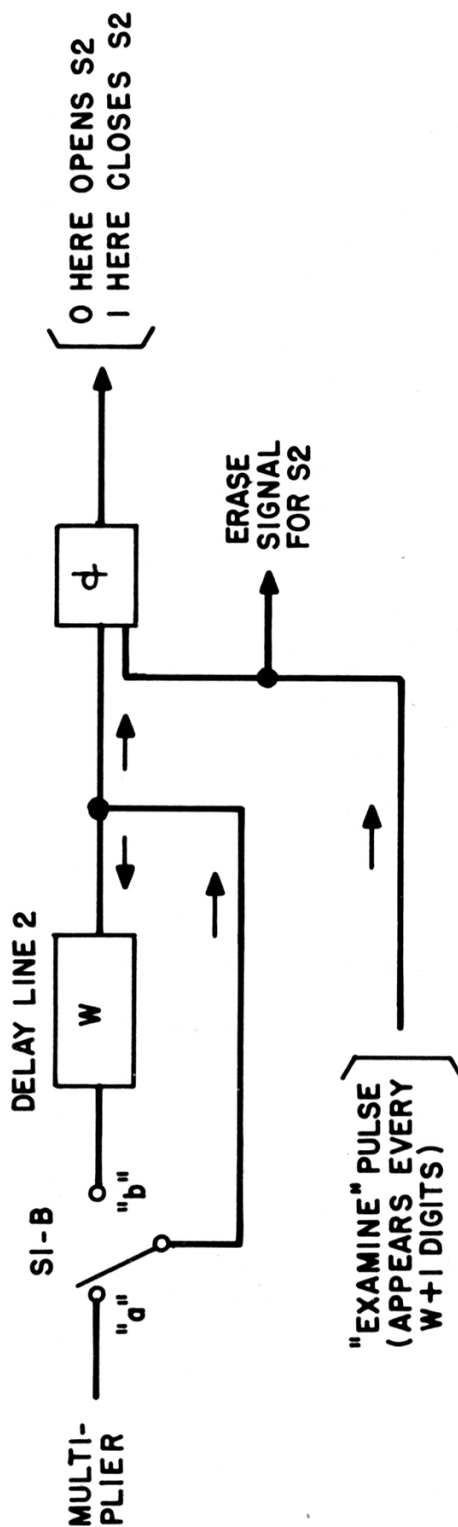
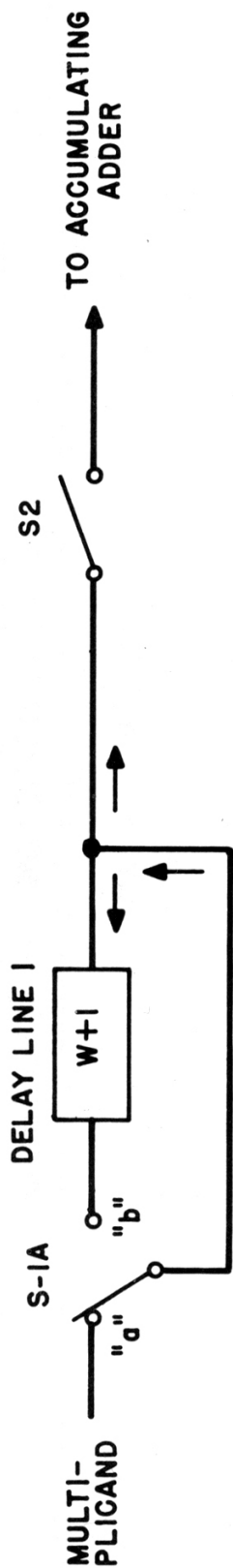


FIGURE 2-II
PARTIAL BLOCK
DIAGRAM OF MULTIPLIER

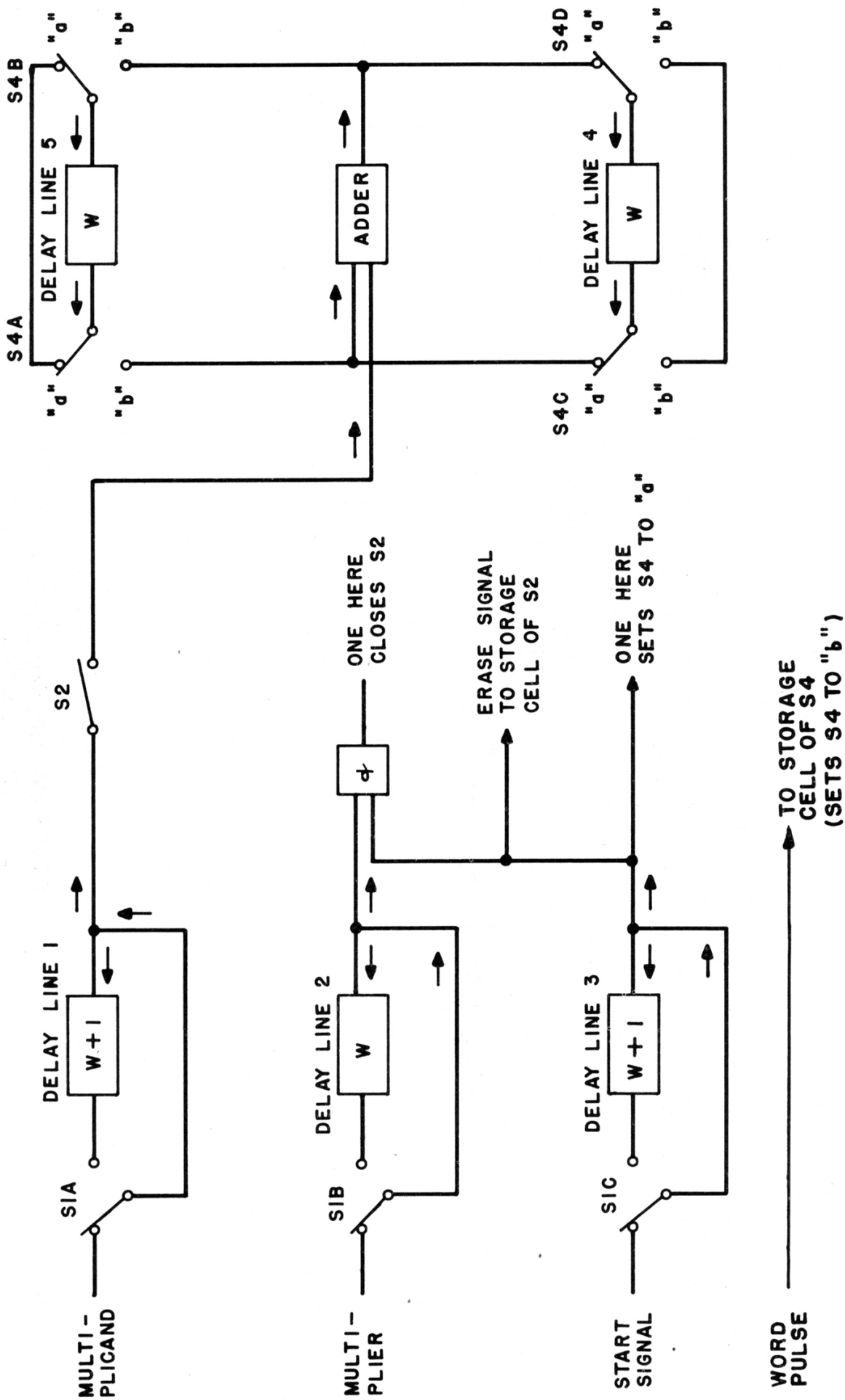


FIGURE 2-12
BLOCK DIAGRAM
OF
MULTIPLIER

MULTIPLICATION OF 1001 BY 1101 IN W=4 SYSTEM																					
← TIME		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
WORD PULSES		1				1				1				1				1			
MULTIPLICAND (DL1)		1	0	0	1		1	0	0	1		1	0	0	1		1	0	0	1	
MULTIPLIER (DL2)		1	1	0	1	1	0	1	1	0	1	1	0	1	0	1	1	0	1	0	1
W+1 PULSES							1					1					1				
POSITION OFS2		← — CLOSED — OPEN — CLOSED — ←																			
FROM S ₂		1	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	1
FROM DL4								1	0			1	0								
FROM DL5		0	1	0	0	0	0			0	0			0	0	0	0				
TO DL4							0				1	1	1				0				
TO DL5		0	1	1	1	0				0	0			0	1	0					
FROM ADDER							0				1	1	1				0				
FROM DL4		0	1	0	1						0			1	0	1					
FROM ADDER		0	1	1	1						0				1	0					
FROM DL5							0						0				0				
POSITION S ₄		b	b	b	b	a	b	a	a	b	a	a	a	b	b	b	a	b	b	b	b

ANSWER = $\overbrace{011}^{DL5} \overbrace{0101}^{DL4}$

FIGURE 2 - 13
EXAMPLE OF
MULTIPLICATION

BINARY DIVISION

DIVIDE 3 (11) BY 8 (1000)

$$\begin{array}{r} 0.011 \\ 1000 \overline{) 11.000} \\ \underline{10\ 00} \\ 1\ 000 \\ \underline{1\ 000} \\ 0 \end{array}$$

DIVIDE 15 (1111) BY 24 (11000)

$$\begin{array}{r} 0000.101 \\ 11000 \overline{) 1111.000} \\ \underline{1100\ 0} \\ 11\ 000 \\ \underline{11\ 000} \\ 0 \end{array}$$

FIGURE 2 - 14
BINARY DIVISION

DIVIDE 3 BY 8

WORD LENGTH = 5 PLACES. 5TH PLACE INDICATES SIGN.

3 =	00011
8 =	01000
ONES COMPL. =	10111
ADD ONE	<u>1</u>
-8 =	11000

CHANGE NUMBERS TO 2W-1 OR 9 DIGIT LENGTH.

3 = 000000011
 8 = 000001000
 -8 = 111111000

DIVISION RULE: IF (2W-1)th (9th) DIGIT OF REMAINDER IS ZERO ADD - DIVISOR; ADD + DIVISOR IF DIGIT IS ONE.

		0.01100
000001000		000000011.00000
ADD - 8		111111000
NOTE 9TH DIGIT → 1	11111011	
AND ADD +8 WITH SHIFT	000001000	
NOTE 9TH DIGIT → 1	11111110	
AND ADD +8 WITH SHIFT	000001000	
NOTE 9TH DIGIT → 0	00000100	
AND ADD -8 WITH SHIFT	111111000	
NOTE 9TH DIGIT → 0	00000000	
AND ADD -8 WITH SHIFT	111111000	
NOTE 9TH DIGIT → 1	111111000	
AND ADD +8 WITH SHIFT	000001000	
NOTE 9TH DIGIT → 1	111111000	

THE QUOTIENT IS THE ONES COMPLEMENT OF THE SUCCESSIVE 9TH DIGITS OF THE REMAINDERS

FIGURE 2 - 15
 SIMPLIFIED
 BINARY DIVISION

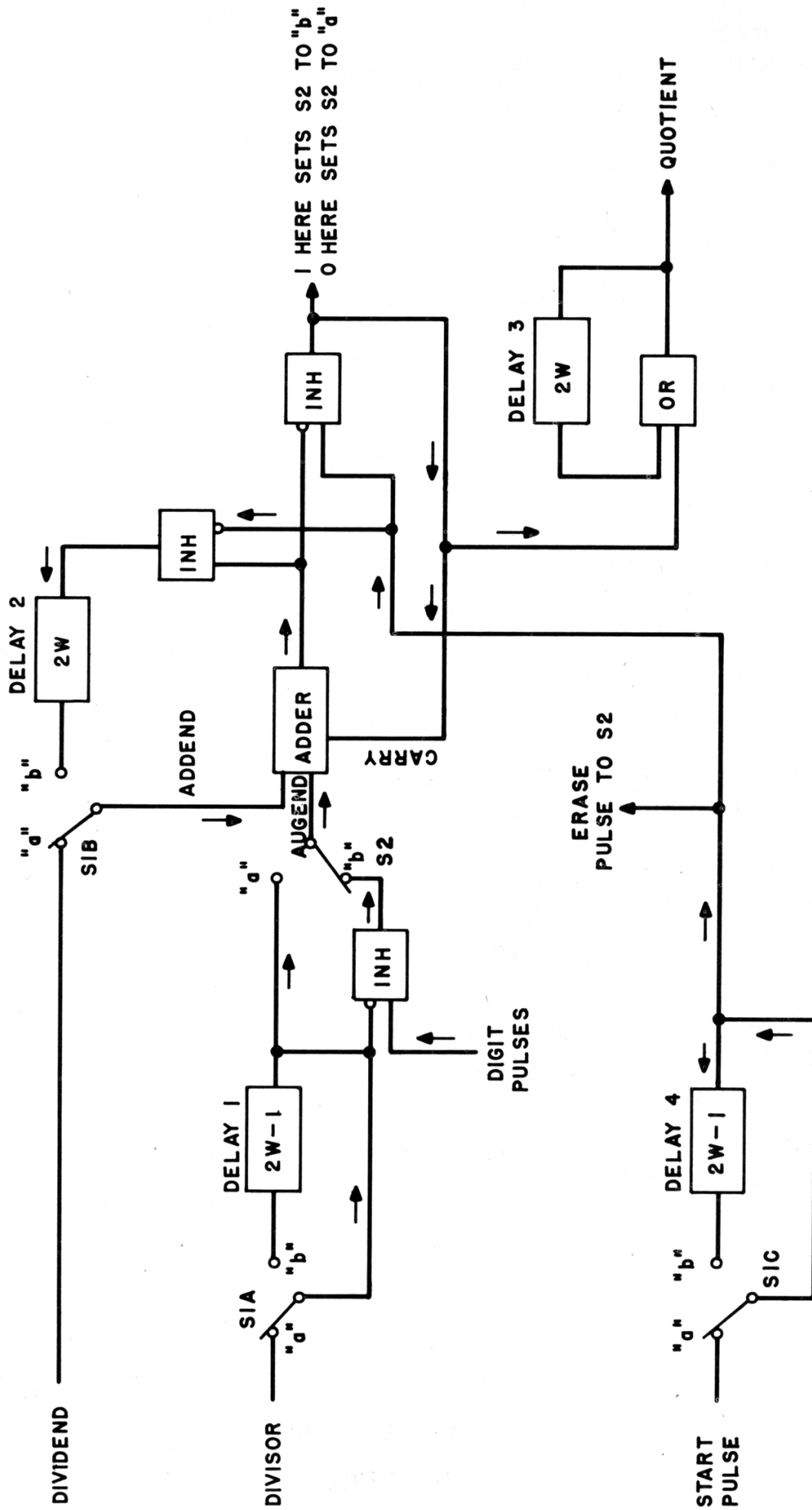


FIGURE 2-16

DIVIDER

BLOCK DIAGRAM

ALGEBRAIC
PROCEDURE

ARITHMETIC
PROCEDURE

FIND \sqrt{x}

STEP 1

MAKE FIRST ESTIMATE h_1 AND
OBTAIN FIRST REMAINDER.

$$R_1 = x - h_1^2$$

STEP 2

MAKE ESTIMATE OF INCREMENT
 h_2 SUCH THAT $h_2(2h_1 + h_2) \leq R_1$
AND COMPUTE SECOND REMAINDER.

$$R_2 = R_1 - h_2(2h_1 + h_2)$$

$$[\text{NOTE: } R_2 = x - (h_1 + h_2)^2]$$

STEP 3

FIND h_3 SUCH THAT
 $h_3 [2(h_1 + h_2) + h_3] \leq R_2$
AND COMPUTE THIRD REMAINDER

$$R_3 = R_2 - h_3 [2(h_1 + h_2) + h_3]$$

$$[\text{NOTE: } R_3 = x - (h_1 + h_2 + h_3)^2]$$

STEP N

$$R_n = R_{n-1} - h_n \left[2 \sum_{j=1}^{j=n-1} h_j + h_n \right]$$

$$\sqrt{x} \approx h_1 + h_2 + h_3 + \dots + h_n$$

FIND $\sqrt{123,904}$

STEP 1

$$h_1 = 300$$

$$\begin{array}{r} 123904 \\ -90000 \\ \hline 33904 = R_1 \end{array}$$

STEP 2

FIND h_2 SUCH THAT

$$h_2(600 + h_2) \leq 33904$$

$$50 \times 600 = 30,000$$

$$\therefore h_2 = 50$$

$$50(600 + 50) = 32,500$$

$$\begin{array}{r} 33904 \\ -32500 \\ \hline 1404 = R_2 \end{array}$$

STEP 3

FIND h_3 SUCH THAT

$$h_3(2 \times 350 + h_3) \leq 1404$$

$$2 \times 700 = 1400$$

$$\text{TRY } h_3 = 2$$

$$2(700 + 2) = 1404$$

$$\begin{array}{r} 1404 \\ -1404 \\ \hline 0000 = R_3 \end{array}$$

$$\therefore (h_1 + h_2 + h_3)^2 = 123,904$$

$$\sqrt{123904} = 352$$

FIGURE 2-17
ALGEBRAIC
JUSTIFICATION OF
SQUARE ROOT
METHOD

FIND SQUARE ROOT 1101001001

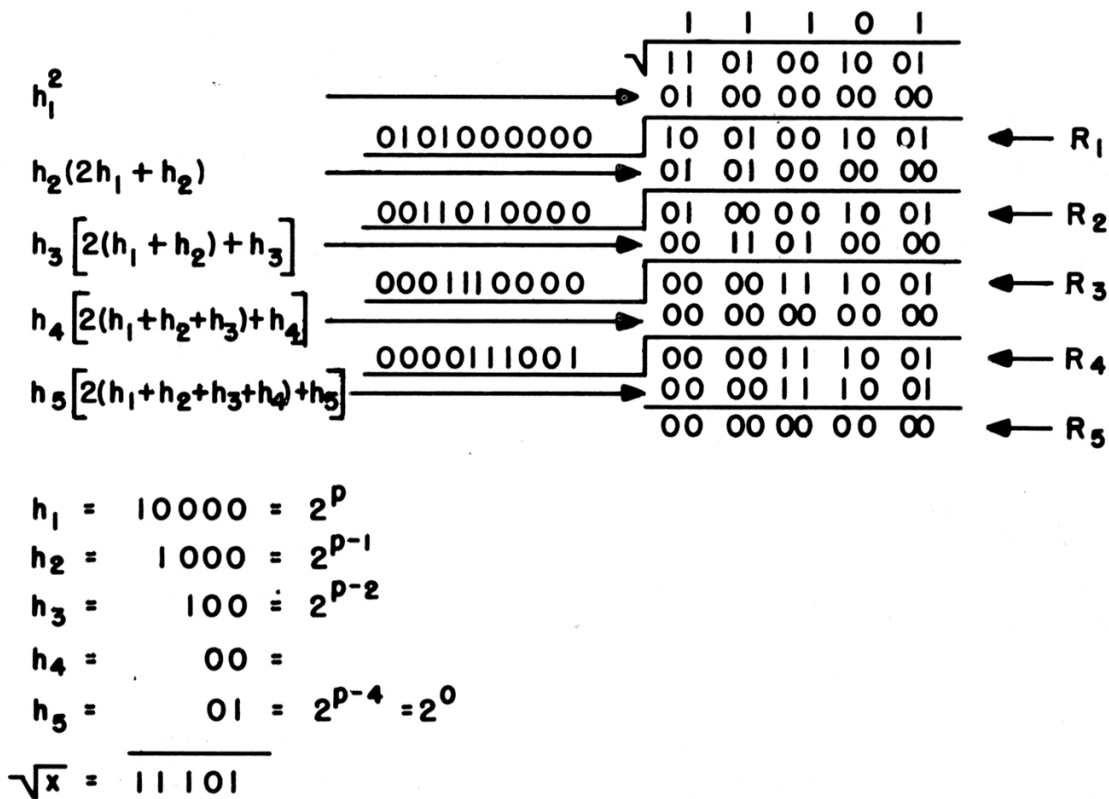
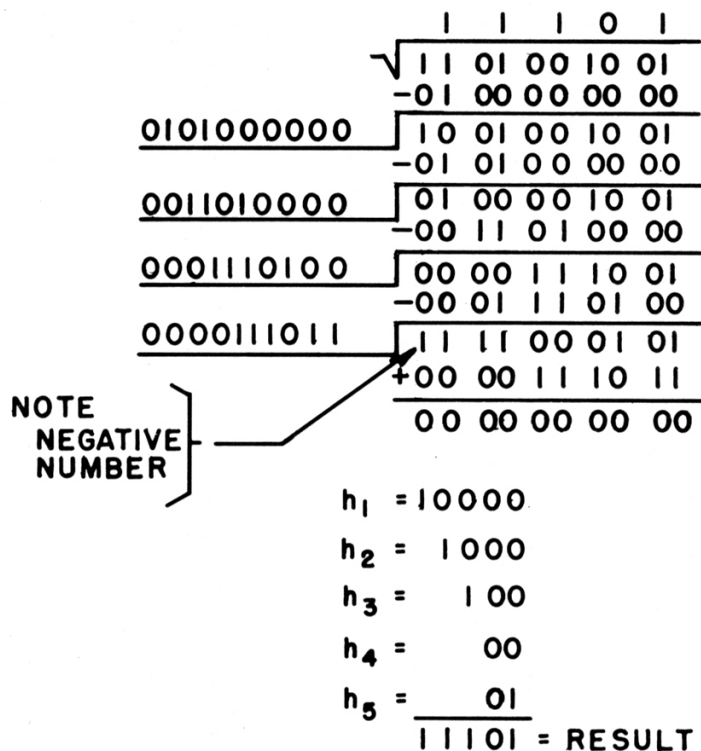


FIGURE 2-18
BINARY SQUARE
ROOTING

EXAMPLE ONE

FIND SQUARE ROOT 1101001001



EXAMPLE TWO

FIND SQUARE ROOT 1001110001

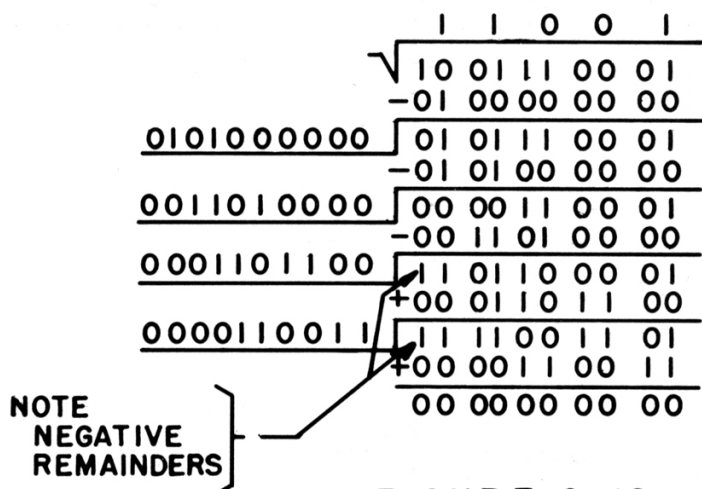


FIGURE 2-19
SIMPLIFIED BINARY
SQUARE ROOTING

FIND SQUARE ROOT OF 1001110001



30 29 28 27 26 25 24 23 22 21	20 19 18 17 16 15 14 13 12 11	10 9 8 7 6 5 4 3 2 1	DIGIT TIME
0 0 0 1 1 0 0 0 1	0 1 0 1 1 0 0 0 1	1 0 0 1 1 0 0 0 1	{ MINUEND OR ADDEND
0 0 1 1 0 1 0 0 0 0	0 1 0 1 0 0 0 0 0 0	0 1 0 0 0 0 0 0 0 0	{ SUBTRAHEND OR AUGEND
1 1 0 1 1 0 0 0 0 1	0 0 0 0 1 1 0 0 0 1	0 1 0 1 1 0 0 0 1	{ REMAINDER OR SUM
0 C ₃	1 C ₂	1 C ₁	{ ANSWER DIGIT
C ₁ C ₂	C ₁		{ REAPPEARANCE OF ANSWER DIGITS



50 49 48 47 46 45 44 43 42 41	40 39 38 37 36 35 34 33 32 31	DIGIT TIME
1 1 1 1 0 0 1 1 0 1	1 1 0 1 1 0 0 0 0 1	{ MINUEND OR ADDEND
0 0 0 0 1 1 0 0 1 1	0 0 0 1 1 0 1 1 0 0	{ SUBTRAHEND OR AUGEND
0 0 0 0 0 0 0 0 0 0	1 1 1 0 0 1 1 0 1	{ REMAINDER OR SUM
1 C ₅	0 C ₄	{ ANSWER DIGIT
C ₁ C ₂ C ₃ C ₄	C ₁ C ₂ C ₃	{ REAPPEARANCE OF ANSWER DIGITS

FIGURE 2 - 20
DETAILS OF
SQUARE ROOT PROCESS

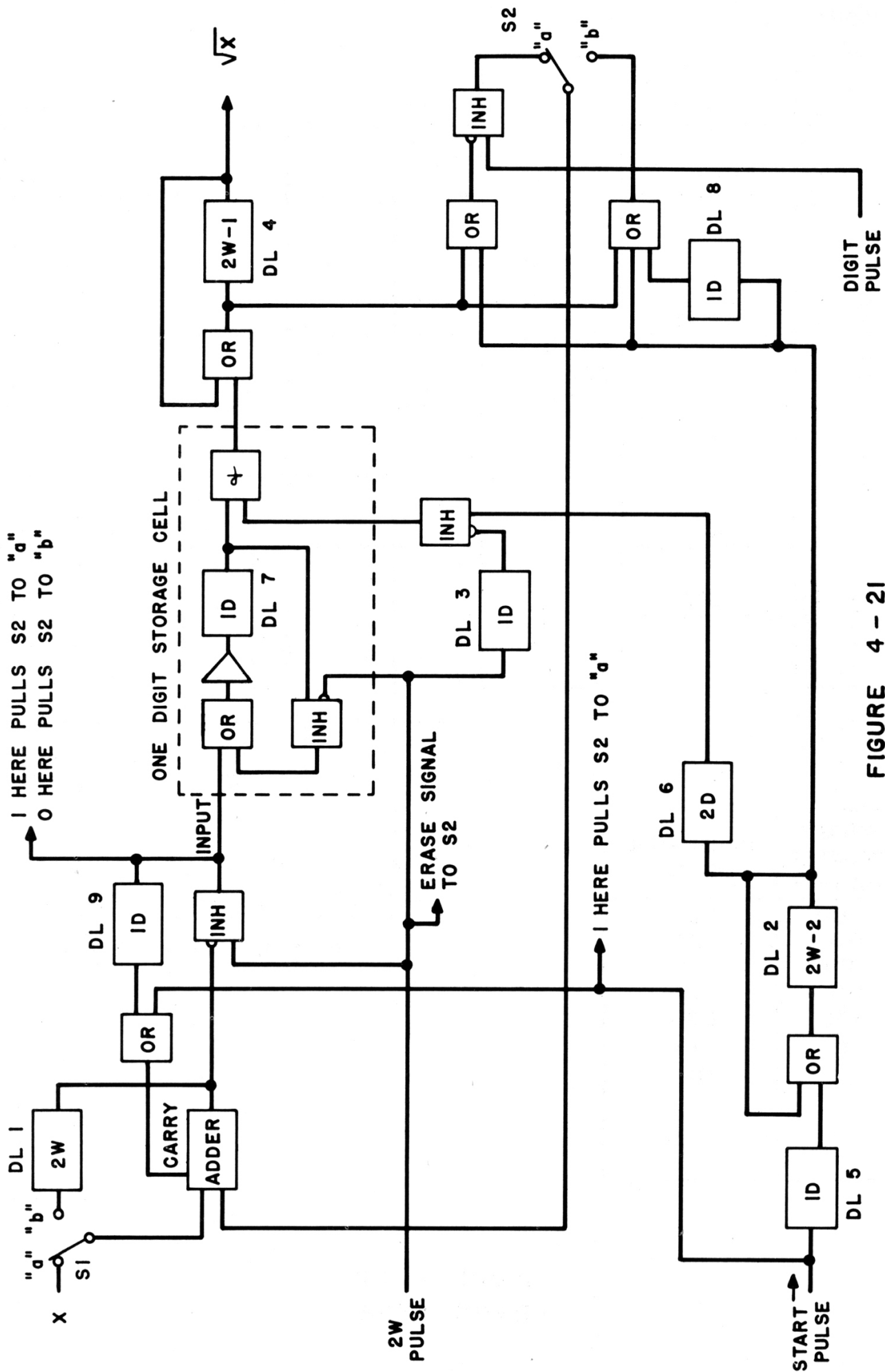


FIGURE 4 - 21
 SQUARE ROOTER
 BLOCK DIAGRAM

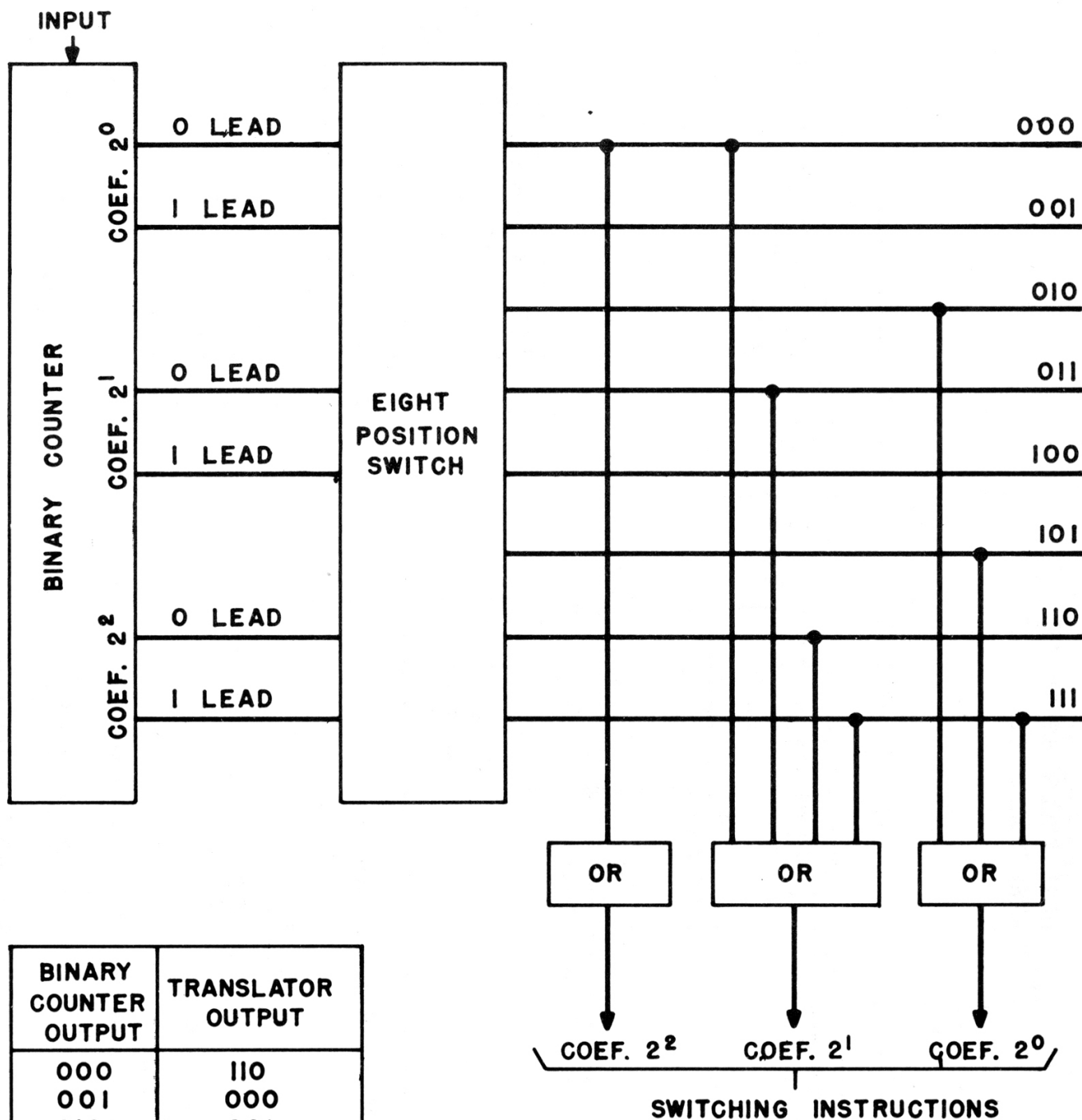


FIGURE 2-22
TRANSLATOR

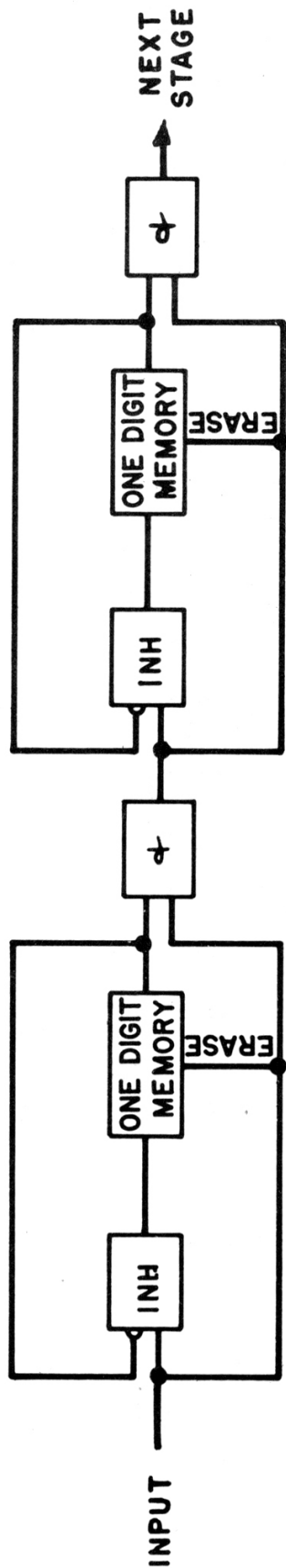
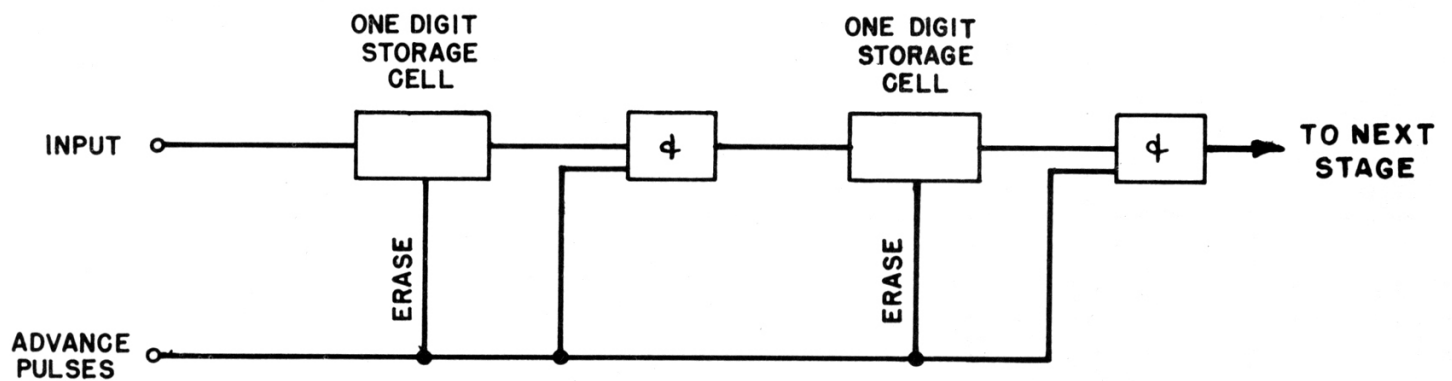


FIGURE 2 - 23
BINARY
COUNTER

REGISTER FOR SERIAL READ OUT (TWO STAGES)



REGISTER FOR PARALLEL READ OUT

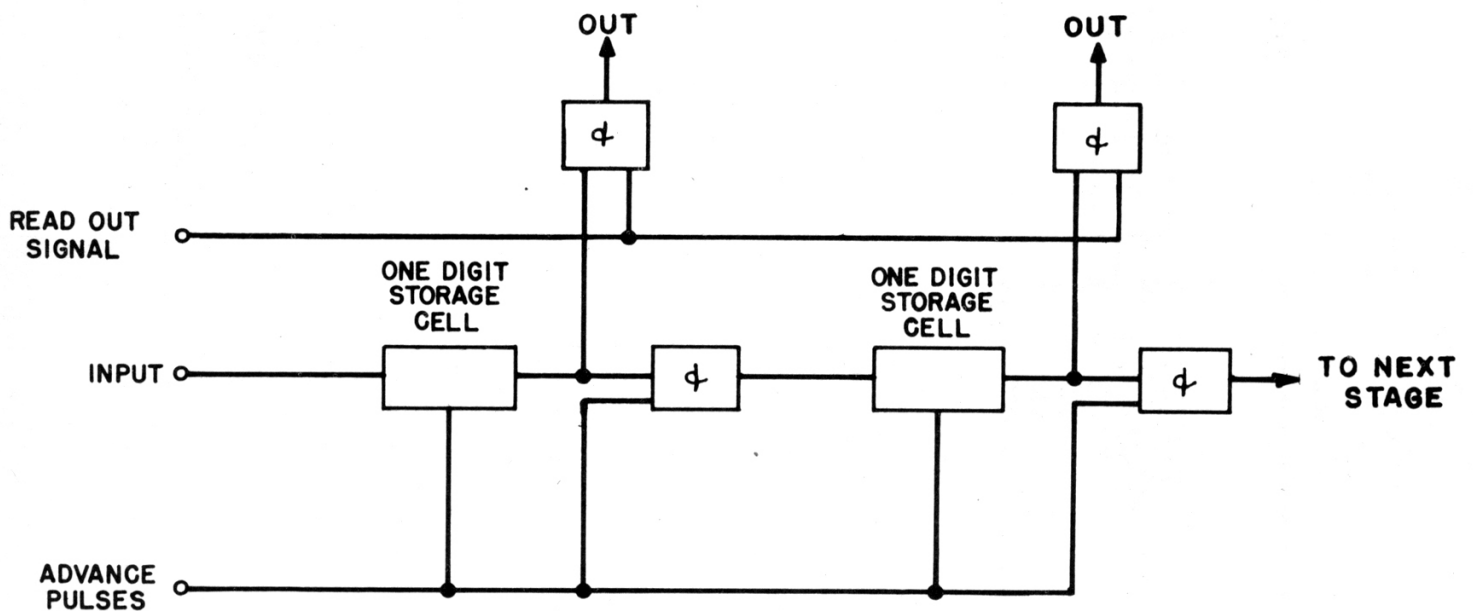


FIGURE 2 - 24
SHIFT REGISTER

A TRANSISTOR BLOCKING OSCILLATOR

3.1 INTRODUCTION

Because the transistor has a much lower input than output impedance, it appeared that a transistor pulse-generator could be designed in which the output is coupled back to the input through an impedance changing transformer. Experiments along these lines show that it is possible to build a transistor blocking oscillator that will work with almost any transistor. Rectangular pulses of less than a microsecond duration are easily generated, and rise times as short as 0.01 microsecond have been observed in 20-volt pulses. Pulse repetition frequencies from the low audio range up to two megacycles have been obtained. Analysis of the circuit reveals that the negative resistance required for oscillation can be obtained even though transistor current gain is less than one.

3.2 BASIC CIRCUITS

The basic circuit is shown in Figure 1A where the transformer couples the inverted collector pulse back to the base at an impedance level comparable to the base impedance. A variation of the circuit is shown in 1B, where the collector voltage is fed back in phase to the emitter. Both circuits oscillate, but most of the work has been done on circuit 1A.

When the oscillator is to be free-running, R (Fig. 1) is returned to a positive voltage in such a way that a constant current of about one milliamperes is supplied to the emitter. If the circuit is to operate only when triggered, R is generally returned to a negative voltage.

3.3 CIRCUIT OPERATION

The circuit operates much like the vacuum tube equivalent. During the "ON" period, the collector voltage is nearly at ground, the base is held negative by the pulse transformer, and the emitter condenser (Fig. 2) is charged negative by the emitter current to a voltage nearly equal to the base voltage. During the "OFF" period, the collector voltage is negative, the base is at ground potential, and the charge left on C holds the emitter at a negative potential.

For purposes of a more detailed discussion, assume that the emitter condenser has been charged negatively and is discharging through R towards a positive voltage. Until the condenser reaches ground potential, the transistor is cut off. When the condenser reaches ground potential, emitter current begins to flow, releasing holes to the collector. The collector current pulls the collector potential up, and transmission through the inverting transformer causes the base to fall in potential which increases the emitter current. This regenerative transition from no emitter current to high current may occur in from one-hundredth of a microsecond to several tenths of a microsecond, depending on the particular transistor. Transistors of the type currently supplied for experimental use have rise times of less than 0.1 microsecond.

During the transition the emitter current (see Fig. 2) is charging C negatively, but as C charges the emitter current decreases because the emitter becomes less positive with respect to the base. At the same time that the emitter current is falling, the collector current required in the transformer to maintain the negative pulse at the base increases because of the low frequency cut-off (or time constant) of the transformer. When the emitter current has fallen to where it no longer releases the holes necessary to support the demanded collector current, the base voltage will rise towards ground which will cause a further decrease in emitter current, and the transistor will regeneratively cut itself off. C is left at a negative potential and begins again to discharge through R towards ground.

The above discussion shows that the recurrence rate is determined by C and the current supplied through R. The pulse duration is determined primarily by the transformer and C, and only in part by the transistor.

In appendix I, an analysis of the circuit is presented on the basis of linear circuit theory.

3.4 EXPERIMENTAL RESULTS

Figure 3 shows an experimental circuit built to develop a trigger pulse in advance of a main pulse, so that the main pulse could be observed on an oscilloscope. Transistor 1 was connected as a free-running blocking oscillator and its output differentiated and delayed 0.15 microseconds to trigger transistor 2.

Using transistor AN2891, the free-running circuit had a pulse duration of 1.5 microseconds, a rise time of 0.15 microseconds, a collector-pulse-amplitude of 30 volts, and developed a 10-volt signal across 560 ohms in the tertiary of the transformer. The 400A crystal was put across the collector winding of the transformer to clip the negative tail that occurs at the end of the pulse when the transformer is not fully loaded down.

The second circuit was tried with 41 transistors and worked with 40, while it was unstable with one. Five of these transistors were of miscellaneous previous history, while thirty-six were loaned from the spares of a matrix switch. Of the latter group of 36, 9 had rise times of 0.03 microseconds or less. The average duration of the pulse was 0.8 microseconds, and the standard deviation was less than 0.1 microseconds.

Photographs were made of the extremely steep wave forms that can be generated. Figure 4 shows the circuit used, and Figure 4A shows the collector output pulse. Figure 4B shows the collector output when C is returned to the collector, rather than ground. This circuit variation has been found to flatten the collector pulse but lengthen the fall time.

In these photographs, one small division equals 0.01 microseconds. Thus the transistor is seen to be capable of generating pulse energy over an extremely wide video band. It may be that in spite of its restricted bandwidth as a linear amplifier, the low inductance of its leads and their very small shunt capacitances may make it a better generator of extremely rapid pulses than the vacuum tube.

3.5 DESIGN OF CIRCUITS

An advantage of the circuit is that its performance is predictable in advance. The selection of the components to obtain the desired results are discussed below:

a. Transformer - For pulses of from one-half to two microseconds duration, two types of transformer cores have been tested. One is a rectangular core of 4-79 Molybdenum Permalloy having a cross-sectional area of 1/16 square inch and overall dimensions of 1 x 1-1/8 inches. The

second core tested is a 3/4 inch ferrite ring with a cross-sectional area of 9/256 square inches. The writer believes that the 0.01 microsecond rise time observed with some transistors might have been even less if better transformers were available.

Some of the factors influencing the selection of the turns ratio are discussed in the appendix. A turns ratios of approximately five to one has been found to give good results with all transistors. Lower ratios do not work with some units.

b. Pulse Duration - The pulse duration, as discussed in paragraph 3, is determined by the transformer low-frequency response, the value of the emitter condenser and in part by the transistor. A 430 mmf condenser and a transformer with three turns in the base winding and 16 in the collector (using the 4-79 Molybdenum Permalloy core previously mentioned) gives a 1/3 microsecond pulse. Using the same core with nine turns in the base and 50 turns in the collector winding, and a 2200 mmf condenser, a duration of 1-1/2 microseconds was obtained.

It should be noted that C can be made so large that the emitter current required to charge it to the base voltage may burn out the transistor.

c. Recurrence Rate - For predictable results, the emitter resistor R should be returned to a large positive voltage (E_e), so that a constant current is supplied to the emitter. If the emitter swings during the pulse in ΔE_e , the recurrence rate will be

$$f_r = \frac{1}{\frac{\Delta E_e}{E_e} RC + \tau}$$

where τ is the pulse duration. This equation has been found to give results as good as could be checked on an oscilloscope. The emitter swing is equal to the base swing and is given approximately by

$$\frac{\Delta E_c}{N}$$

where ΔE_c is the collector swing, and N is the transformer turns ratio. If the collector winding is returned to a battery of E_c volts, and N is three or more, the swing in collector voltage will almost equal the battery voltage and will be very stable. An approximation to the recurrence rate is, therefore, given by

$$f_r \approx \frac{1}{\frac{E_c}{E_e} \frac{RC}{N} + \tau}$$

Where stability of frequency is desired, it is important to supply a constant E_c , rather than obtain it from a series resistor. Six switching transistors were tried in a circuit designed, according to the above equation, to have a period of 14.5 microseconds. The actual periods were measured to be 14, 12, 12.5, 12.5, 12.5 and 14 microseconds.

d. Triggered Oscillator - If the emitter is returned to a negative voltage, a pulse will be obtained only when the circuit is triggered (usually through an auxiliary winding of the transformer). When rapid triggering rates were desired, the emitter resistor R was made 1200 ohms and returned to -1.5 volts. When R and the emitter condenser are both made small, the maximum triggering rate as well as the pulse duration will be influenced by the low frequency cut-off of the transformer.

3.6 CONCLUSIONS

A new transistor circuit has been described whose characteristics are stable and almost independent of the transistor characteristics. Because of its stable and circuit-controlled recurrence frequency, it should be useful as a frequency dividing device. Since it can be operated at a megacycle rate, it should be useful wherever fast powerful pulses are required. The writer is chiefly interested in the device as a regenerative amplifier for digital computer applications.

APPENDIX

ANALYSIS OF TRANSISTOR BLOCKING OSCILLATOR

Analysis of the impedance (R_i) shown at the emitter of the blocking oscillator shows a negative resistance of the series type and the magnitude of this negative resistance may be taken as some evidence of the performance of the circuit as an oscillator. Referring to Figure 5, we may write the following equations (assuming that the transformer is ideal and inverting with a turns ratio n).

In Mesh I

$$i_e(R_e + R_b) - i_c R_b = E - e_b \quad (1)$$

and in Mesh II

$$- i_e(R_b + R_m) + i_c (R_b + R_c) = e_b (n + 1) \quad (2)$$

Since the transformer is assumed to be ideal, we may write

$$i_c = \frac{i_e - i_c}{n} \text{ or } i_c = \frac{i_e}{n+1} \quad (3)$$

Substituting (3) in (1) and (2) gives

$$i_e \left(R_e + \frac{n}{n+1} R_b \right) + e_b = E \quad (4)$$

and

$$- i_e \left(R_m - \frac{R_c}{n+1} + \frac{R_b n}{n+1} \right) - e_b (n + 1) = 0 \quad (5)$$

which can be solved for

$$\frac{E}{i_e} = R_i = - \frac{R_m}{n+1} + \frac{R_c}{(n+1)^2} + R_b \left(\frac{n}{n+1} \right)^2 + R_e \quad (6)$$

If one tries to maximize R_i by varying n , it is found that

$$n_{\text{opt}} = \frac{2(R_c - R_b)}{(R_m - 2R_b)} - 1 \quad (7)$$

or

$$n_{\text{opt}} \approx \frac{2R_c}{R_m} - 1$$

This shows that if R_m/R_c is large, the transformer should not invert in order to maximize R_i .

If $n = \frac{2R_c}{R_m} - 1$ is substituted in (6), we obtain

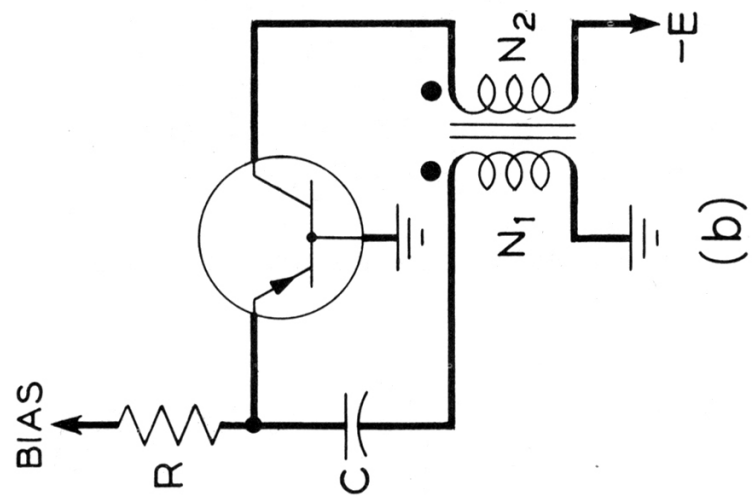
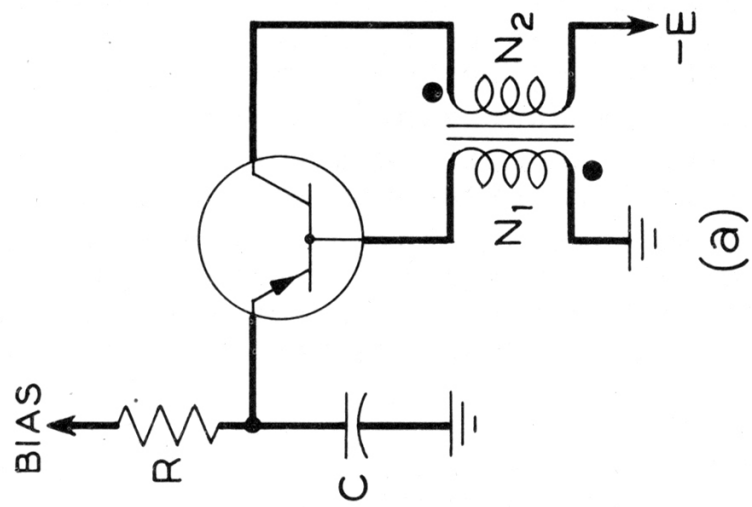
$$R_i = -\frac{R_m}{4} \frac{R_m}{R_c} + R_e + R_b \left(1 - \frac{R_m}{2R_c}\right)^2 \quad (8)$$

which shows that a negative resistance can be obtained when R_m is less than R_c .

When choosing the transformer, one has to consider the values of R_m and R_c over the entire range of collector current. A negative resistance is desired over as large a portion of the collector current curve as possible.* At the boundaries of the collector current range, R_m will be less than R_c , and this suggests that one ought to make the transformer inverting and with a turns ratio of three or so to obtain regeneration even when $R_m = 1/2 R_c$. Experience to date has shown that any lower turns ratio is not desirable, but no upper limit has been investigated chiefly because the performance of the circuit is not very sensitive with regard to n , except in the respects mentioned in paragraph 5.

* In order to get the maximum possible collector current swing and minimum voltage rise time.

TRANSISTOR BLOCKING OSCILLATOR CIRCUITS



TYPICAL WAVE FORMS IN BLOCKING OSCILLATOR

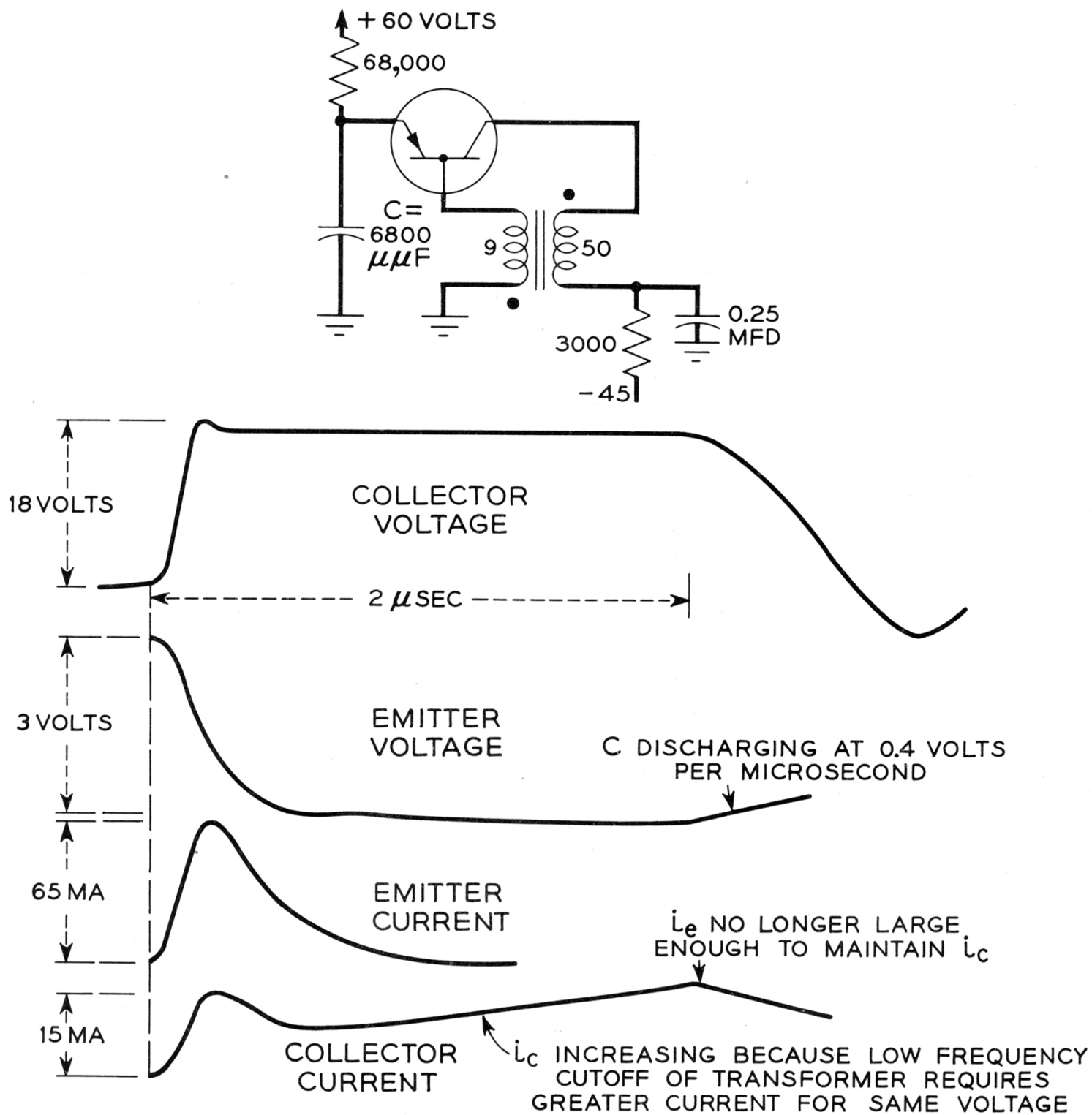
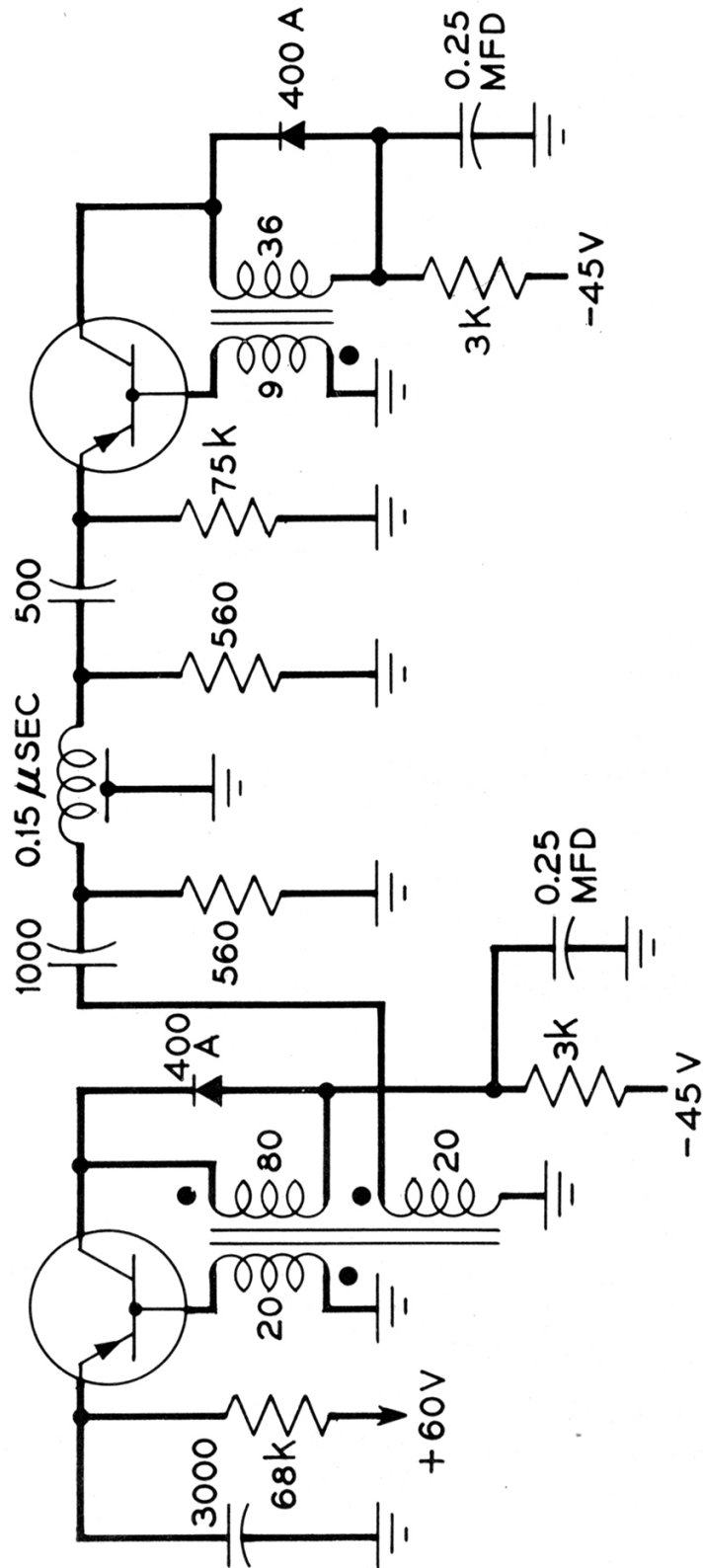


FIG. 2

TEST CIRCUIT FOR OBSERVING MAIN OSCILLATOR PULSE

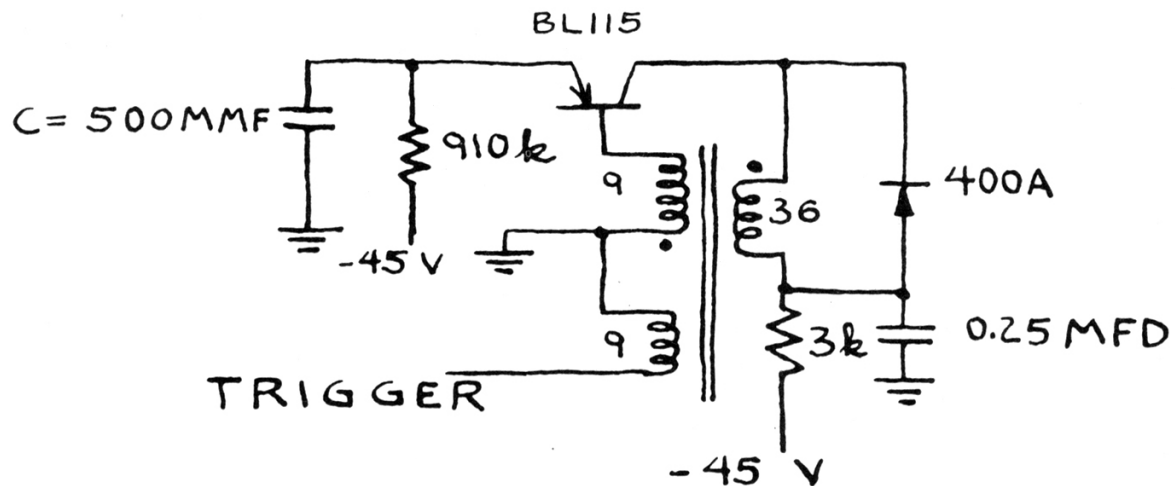


NO.1

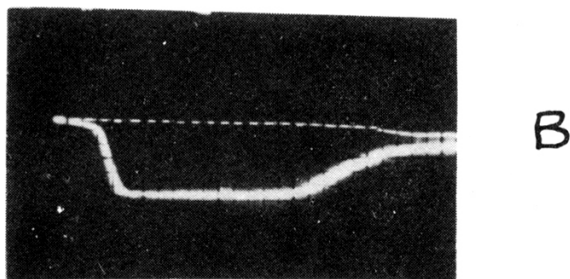
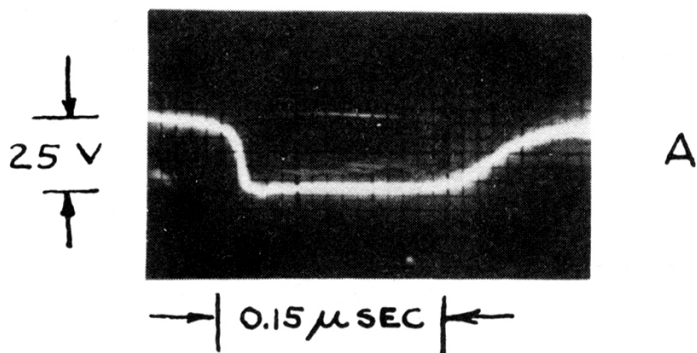
NO.2

FIG. 3

STEEP WAVE FRONTS IN TRANSISTOR BLOCKING OSCILLATOR



COLLECTOR WAVEFORMS
(INVERTED)



C RETURNED TO COLLECTOR

FIGURE 4

EQUIVALENT CIRCUIT OF TRANSISTOR BLOCKING OSCILLATOR

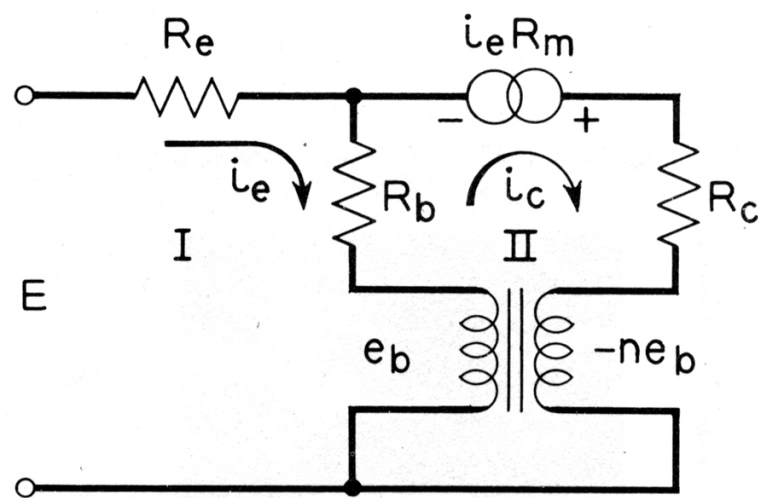


FIG. 5

COUNTING DOWN WITH BLOCKING

OSCILLATORS

4.1 INTRODUCTION

In serial computers a word pulse is required to mark the beginning of each new word or number. For this project 16 digit words were desired at a digit rate of one megacycle. The word-pulse generator therefore is a frequency divider having a one megacycle input and a 62.5 kc output. A chain of four blocking oscillators has been used for the frequency division.

4.2 SCHEMATIC

The schematic of the word-pulse generator is shown in figure 4-1 and in figure 4-2 the emitter and collector wave forms are shown. The first stage was set to free run at about 350 kc. The saw-tooth at the emitter caused by the discharge of C1 through R3 has superimposed upon it the one megacycle clock signal. This signal synchronizes the firing of the first stage at 500 kc as can be seen from figure 4-2. A portion of the output of the first stage is coupled to the second stage and synchronizes it at 250 kc. The third stage is similarly synchronized at 125 kc and the fourth at 62.5 kc.

The output of the fourth stage is used to synchronize test oscilloscopes. It also drives an output amplifier of the type described in paragraph 5. This amplifier standardizes the duration of the word pulse at 1/2 microsecond.

Front and back views of the unit are shown on photograph 192402. One of the coaxial cables shown carries the clock signal. A second cable carries a synchronizing signal to test oscilloscopes and a third cable carries the word pulse to the computer.

4.3 SUMMARY

The word pulse generator described herein has been operated since January of 1951 without transistor replacements. It has a total battery drain of only 80 milliwatts.

WORD - PULSE GENERATOR

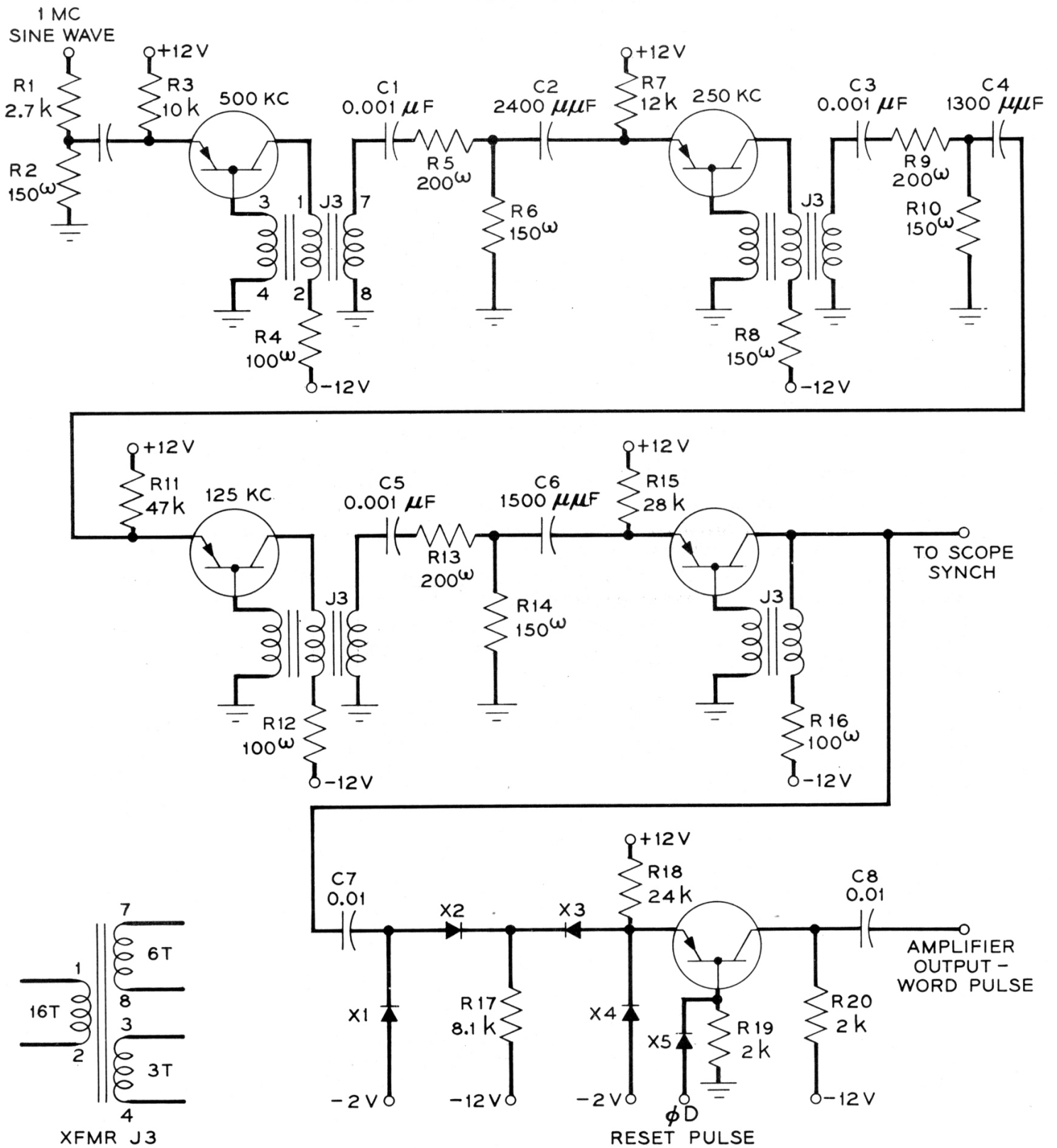


FIG. 4-1

WAVEFORMS IN WORD-PULSE GENERATOR

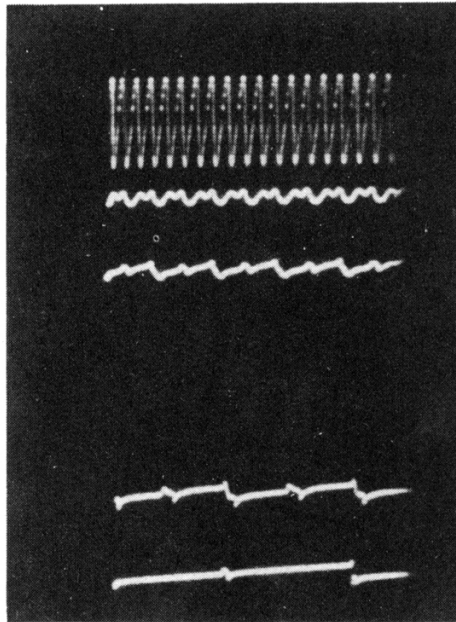
ONE MEGACYCLE

1 ST EMITTER

2 ND EMITTER

3 RD EMITTER

4 TH EMITTER



EMITTER WAVEFORMS

ONE MEGACYCLE

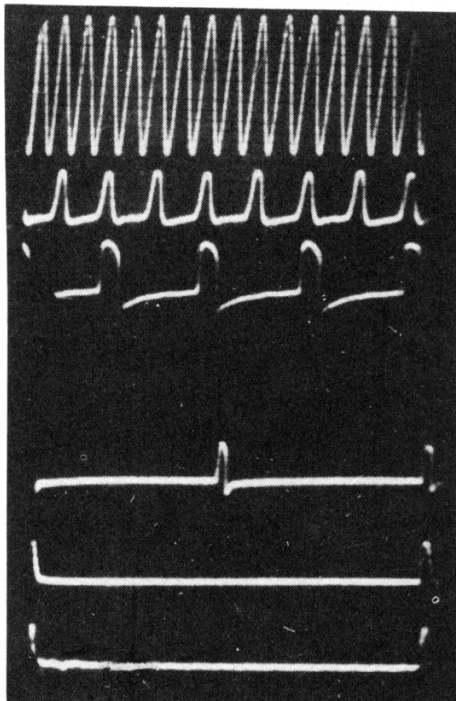
1 ST COLLECTOR

2 ND COLLECTOR

3 RD COLLECTOR

4 TH COLLECTOR

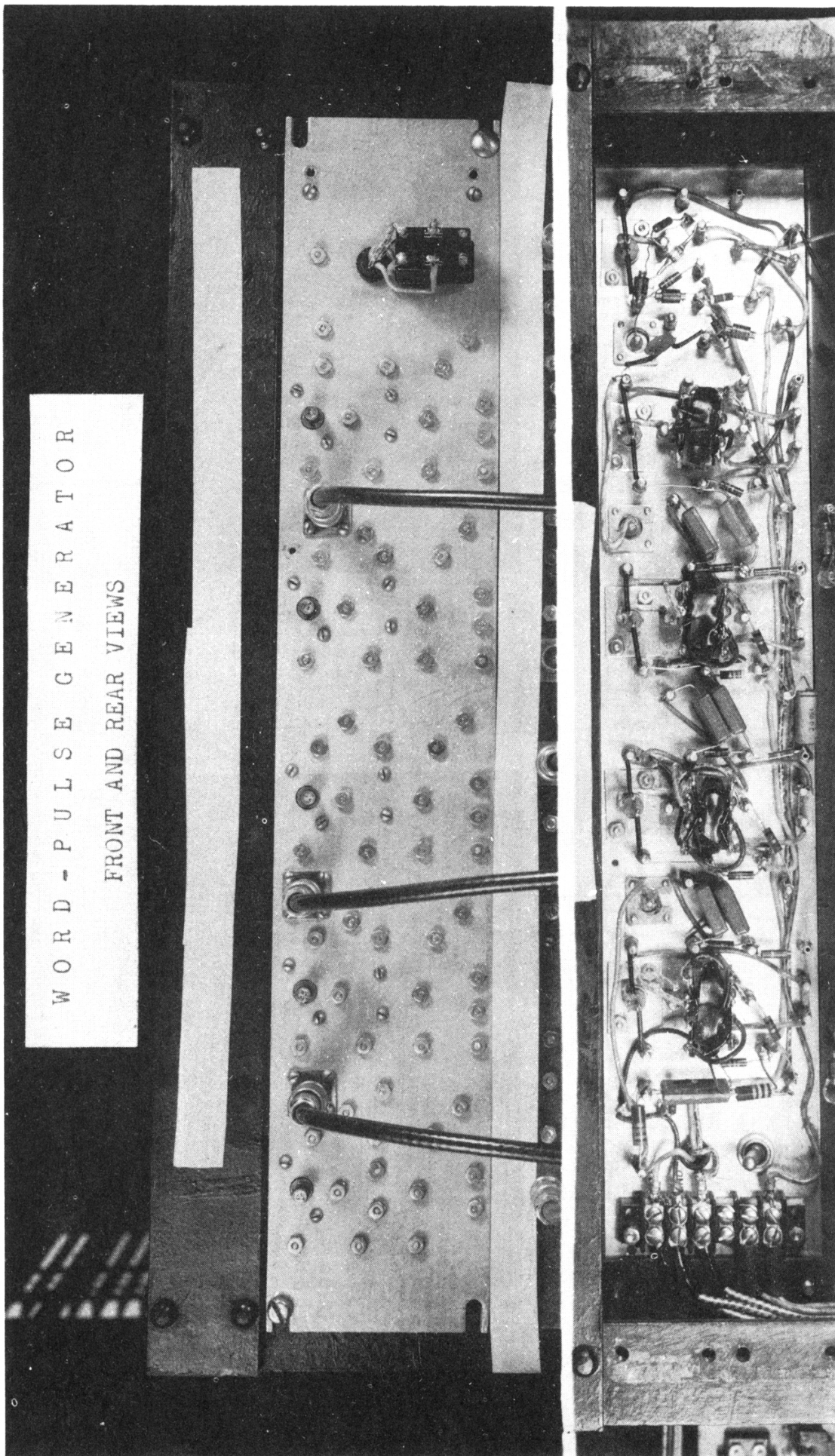
OUTPUT



COLLECTOR WAVEFORMS

FIGURE 4-2

WORD - PULSE GENERATOR
FRONT AND REAR VIEWS



BASIC TRANSISTOR AMPLIFIER

5.1 INTRODUCTION

A good vacuum tube may not have serious transit time limitations upon its use at frequencies below 1000 megacycles, but the parasitic impedances of the same vacuum tube will limit its use in wide-band circuits to band widths of about 20 megacycles. High-speed transistors are limited by transit time considerations to frequencies below about 50 megacycles, but the parasitic limits are at frequencies above the transit-time limits, and for that reason the slow "hole" of transistor electronics may be a better carrier for the production or amplification of high-speed pulses than is the much faster electron of vacuum tube electronics. The M1734 type transistor in the circuit to be described is a fast pulse amplifier competitive with vacuum tubes in high-speed switching systems. In the applications described one may say that a vacuum tube would be a poor transistor substitute.

5.2 INPUT CHARACTERISTIC OF THE TRANSISTOR

Figure 1 illustrates the negative input impedance of the transistor for a current gain (α) greater than 1 and a high base impedance. Figure 2 shows a typical characteristic for an M1734 transistor.

The relationships shown on Figure 1 for the valley voltage and current are approximate and based on a number of assumptions about the relative magnitudes of the transistor parameters. The interested reader is advised to start with the "broken-line" assumptions of Mr. B. G. Farley and derive his own relationships. The broken line assumptions are:

1. R_e , the emitter impedance, is high and constant (comparable to the back impedance of a diode) when negative emitter current flows and low and constant (comparable to the forward impedance of a diode) when positive emitter current flows.
2. R_b , the base impedance, is constant.
3. R_c , the collector impedance, is high and constant for negative or positive emitter currents unless the unit is saturated, in which case the collector impedance drops to a constant value of the same order as the emitter impedance.

4. R_m , the mutual impedance, is zero for negative emitter current, constant and high for positive emitter current unless the unit is saturated, in which case R_m is zero.

The most significant feature of the characteristic is the peak voltage; the voltage, that is, at which the input resistance becomes negative. The peak voltage is generally negative and the peak point is reached after the current gain becomes greater than 1, which is generally assumed to occur when the emitter current ceases to be negative and becomes positive. There is some evidence that the peak point may not be reached until the emitter current is quite positive. In any event, the peak point is a first-order effect of base impedance and the collector current that flows when the emitter current is zero. In the M1734 transistor efforts are being made to hold the peak point between 0 and -1/2 volt for a transistor with no external base impedance and a collector voltage of -8 volts*.

Another significant point on the emitter characteristic is the valley point, the point at which the transistor saturates. As the emitter current is increased, the collector current increases at a more rapid rate (if $\alpha > 1$) and the resulting base current will carry the internal emitter-base-collector node negative. At the same time the collector current will carry the external collector terminal in a positive direction towards ground (if $R_1 > 0$). When the internal node has fallen to a voltage near that of the collector terminal, the valley point has been reached and the transistor is said to be saturated. The transistor has in effect become a passive network because the holes emitted at the emitter have reduced the effective collector impedance to a minimum value and R_m has therefore been made zero. Further increments in the emitter current will divide between the base and collector circuits in accordance with their impedance levels, and, as seen in Figures 1 and 2, will require that the emitter move positive.

The peak point may be compared to the cut-off point of a vacuum tube, while the valley point is somewhat like the saturation point that is reached in a vacuum tube circuit when the plate voltage has fallen to the cathode voltage. Those working with conditionally stable units must grow accustomed to the cut-off being above the saturation point.

*Various arrangements have been described to make the peak point independent of the external base impedance. These circuit techniques cannot be used to nullify the effect of the internal base impedance.

5.3 ELEMENTARY CIRCUIT

An elementary circuit used to test the pulse performance of transistors is shown in Figure 3. The 1-megacycle sine wave applied to diode X1 carries the emitter positive towards the peak point. When the peak point is exceeded, X1 cuts-off and a current determined by R1 will flow in the emitter circuit. In the circuit shown, the current will be approximately 2 milliamperes and will cause the emitter to go negative along a path that depends upon the emitter capacitance to ground and the bandwidth of the transistor. In any event, the path proceeds either directly or circuitously towards the intersection of the load line of R1 with the emitter v-i characteristic displayed in Figure 1. If the intersection of the two load lines lies between the peak and valley points (a negative resistance region) the unit will oscillate provided the stray capacitance from emitter to ground is large or the bandwidth of the transistor is very wide. If the intersection is at a current greater than the valley current (a positive resistance region) the circuit will rest at a constant emitter voltage below the peak voltage as long as the input sine wave is positive. When the input voltage falls below the emitter voltage, diode X1 conducts and pulls the emitter negative. When the emitter falls below the valley voltage, the emitter current changes from a value greater than the valley current to a value less than the peak current and the transistor remains a high impedance until the input rises once more to a value greater than the peak voltage.

The ratio of i_c to i_e , for $i_e = 2$ ma, as a function of time, has been defined as the pulse alpha; satisfactory M1734 units are expected to have a pulse alpha greater than 1.75 after 0.1 microseconds. Some units develop the required alpha in one or two hundredths of a microsecond and the excellent rise and fall time in the wave form shown in Figure 2 is typical of the M1734 transistor.

5.4 REGENERATIVE AMPLIFIER CIRCUIT

In the circuit of Figure 3, the over-all current gain* is limited to be of the same order as the current gain of the transistor. The current gain can be increased by the addition of diode X2 as in Figure 4. Diode X2 is returned

* Defined as the ratio of the collector of current that flows when the circuit has reached its stable high-current state to the input current required to trigger the circuit.

to a voltage slightly more negative than the peak voltage. Resistors R_1 and R_2 are chosen so that the emitter will rest (when there is no emitter current) at a voltage below the bias on X_2 . This is point A in Figure 4. When the input goes above the peak point, diodes X_1 and X_2 will be cut off and the current set by R_1 will start to flow into the emitter. Because of the negative input impedance the positive emitter current causes the emitter voltage to fall towards C. If the negative resistance is high enough and the unit has sufficient high frequency gain the emitter current will snap out to point B. The circuit will then stay locked up at B indefinitely unless the emitter is pulled below the valley point C or the base is pushed positive. Note that because of the negative impedance at the emitter, the load line can be switched from the high impedance offered by R_2 to the low impedance offered by X_2 when conducting. This gives the circuit a large current gain at the emitter. The emitter current is multiplied by the alpha of the transistor to give a practical current gain at the collector of the order of 20. The minimum triggering current will be influenced by the slope of the curve between point A and C. It may be noted in this connection that if the load line of R_1 does not intersect the load line of X_2 before it intersects the load line of the transistor, in some cases (presumably those involving transistors with restricted bandwidths) the transistor will get "hung up" on the negative impedance portion of the characteristic and the collector signal will be very small.

The above circuit is actually a flip-flop rather than an amplifier. In order to make it an amplifier it is customary to replace diode X_2 with a capacitor. When the emitter current has snapped out to line DC, the capacitor charges down line DC. When the emitter voltage reaches the valley point the current snaps to the low-current state, the capacitor discharges to A, and the unit locks at the low-current state. Thus, the circuit develops an output pulse in return for each input trigger. Two disadvantages of using a condenser to provide automatic shut off in high-speed applications are discussed below. One disadvantage is that the duration of the output pulse depends upon the slope of the transistor characteristic between points C and D. Another disadvantage is that in triggering the circuit, the condenser must be charged from voltage A to the peak

point. This means that if significant delays are to be avoided in high-speed applications, a larger triggering current is required than when diode X2 is used. The circuit shown in Figure 4, can be triggered by a quarter of a milliampere without delays significant to a computer operating at a megacycle rate. (A disadvantage of the circuit of Figure 4 is that it does require a reset pulse.)

Turning off the circuit shown in Figure 4 by a voltage applied at the emitter is extremely difficult since the emitter has to be pulled negative to the valley voltage and the voltage drop has to be developed across the low impedance of the conducting diode X2. However, the circuit can be shut off by a positive reset pulse applied at the base of the transistor through diode X3. It will be seen that the transistor can go to its high current state in this circuit only when the reset pulse is not present and will always be driven back to the low-current state by the next reset pulse applied to the base. Therefore, the onset and the duration of the input pulse is under the control of the reset pulse and is to a degree independent of the transistor, the shape of the input pulse, and the circuit parameters.

This feature makes it a very simple matter to obtain the rigid synchronism required in a serial computer or switching system. Sine-wave clock signals are applied to the bases of the transistor amplifiers through diodes. The phase of the signal fed to the base is chosen so that the base will fall to ground just after the latest time at which the input pulse, if present at all, could have risen. Then the output, if any, will be in synchronism with the clock and not the input. The circuit is therefore a pulse standardizer as well as an amplifier.

These matters may be made clearer by reference to Figure 5. Note that a collector pulse is not produced by a base pulse alone. Only the signal at the emitter can produce an output, and it can produce a signal only during intervals set by the base or clock signal. Diode X4 has been added to the base circuit in order to present a high base impedance when the transistor base is driven positive and to present a low impedance when the transistor is triggered. R4 is added to provide a path for discharging stray capacities. The type of load shown in Figure 5 provides d-c restoration of the signal so that the pulse going into the next diode network

will always start at -2 volts. The load has another purpose in that the conducting diode X5 provides a very low load impedance for the transistor when it first starts to flip to the high current state. This speeds up the regenerative operation. Once the collector voltage has risen appreciably, diode X5 is cut off.

It may also be mentioned that the circuit can be used for indefinite storage by holding back the base pulse until the stored data is to be removed from the circuit. Difficulties encountered with the circuit are described in a later paragraph.

5.5 SOME APPLICATIONS

In Section II "Catalog of Block Diagrams" an extensive group of block diagrams were presented in which all logic operations were to be performed in passive diode circuits and active elements were used only as gain-producing devices to make up for attenuation in the diode circuits. The amplifier circuit described in Paragraph 4 is a circuit recommended for such an application.

Figure 6 shows three common logic circuits. The bottom circuit has an output whenever at least one of its three inputs are energized. The middle circuit will develop an output whenever at least two of its three inputs are energized. The top circuit has an output only if all three of its inputs are energized. Note that the same regenerative amplifier circuit is used in each case.

The top photograph of Figure 7 shows three trains of input pulses; the bottom photograph shows the corresponding outputs of the circuits of Figure 6. The reader can check the operation of the circuits by casting his gaze vertically upwards and downwards across the two photographs to see that the indicated discriminations have been made at each pulse period. As is the case with all the waveforms shown in this memorandum, the width of each pulse represents one-half a microsecond.

Another common logic operation is that of inhibition. A three-terminal and-circuit to which an inhibitor terminal has been added is shown in Figure 8. This circuit has an output only when all three and-inputs are present and the

inhibitor pulse is not. The inhibiting pulse is applied to the base and in effect fills in the blanks in the clock pulses (which, otherwise, would leave the transistor ready to be operated). A complete binary adder has been built using the circuits described in this paragraph and has been operated for over a month at a megacycle rate.

5.6 DIFFICULTIES

The one major difficulty that has been encountered in this project is that some M1734 transistors do not work in the circuit, and it is not always apparent what the basic differences are between a unit that works and one that doesn't. In a group of 42 M1734 transistors recently received, 37 worked in the circuit of Figure 5 and 5 didn't. Of the 37 which worked, some are considered marginal.

In testing units for operation in this type of circuit three voltages are measured. In the circuit of Figure 5, the bias on X2 is made variable. The bias voltage is set at -4 and then gradually brought up towards ground. At first the output will not be a half-microsecond square pulse but will be a packet of sawteeth each lasting about 0.1 microsecond, with the packet lasting a half microsecond. This indicates that the bias on X2 is more negative than the valley voltage. As the bias is carried towards ground, the packet will become a square wave, indicating that the transistor is sticking in a high current state until reset by the base pulse. This means that the load line of X2 is intersecting line CD (see Figure 4) at a voltage more positive than the valley voltage. The voltage at which the square wave is first obtained is called E_1 , (a measure of the valley point). As the bias on X2 is carried closer to ground, it may occur that an output pulse is developed at the end of every base pulse regardless of whether or not an emitter trigger has been received. This voltage is called E_2 and is taken as a measure of the peak point, since the fact that the circuit "fires" at the end of every base pulse indicates that the load line of X2 does not intersect the emitter characteristic in the negative current region. Since, in the absence of an emitter input, the emitter rests at a voltage more negative than the bias on X2, E_2 is more positive than the peak voltage. The bias on X2 is then lowered and the voltage E_3 is noted at which the circuit responds only when there is an emitter trigger. E_3 is generally quite near E_2 if it is much below E_2 hole storage troubles are suspected.

The effects of hole storage are apparent in the positive pips on the trailing edges of almost all of the wave forms. The effect is clear in Figure 5. Note that the collector voltage goes up to (and in some cases above) the emitter voltage before the base pulse succeeds in resetting the transistor. This is not due to a lack of amplitude in the base pulse but results from the fact that the collector remains a low impedance circuit until all of the stored holes have been cleared out.

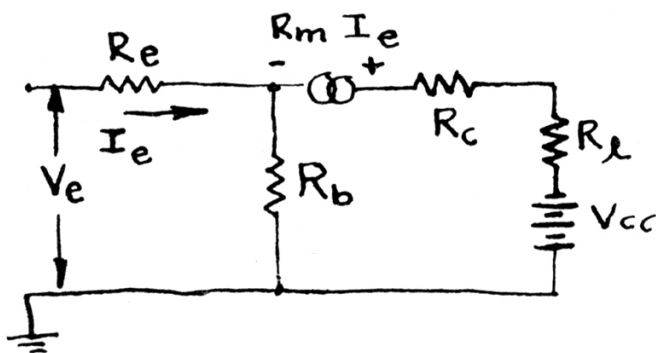
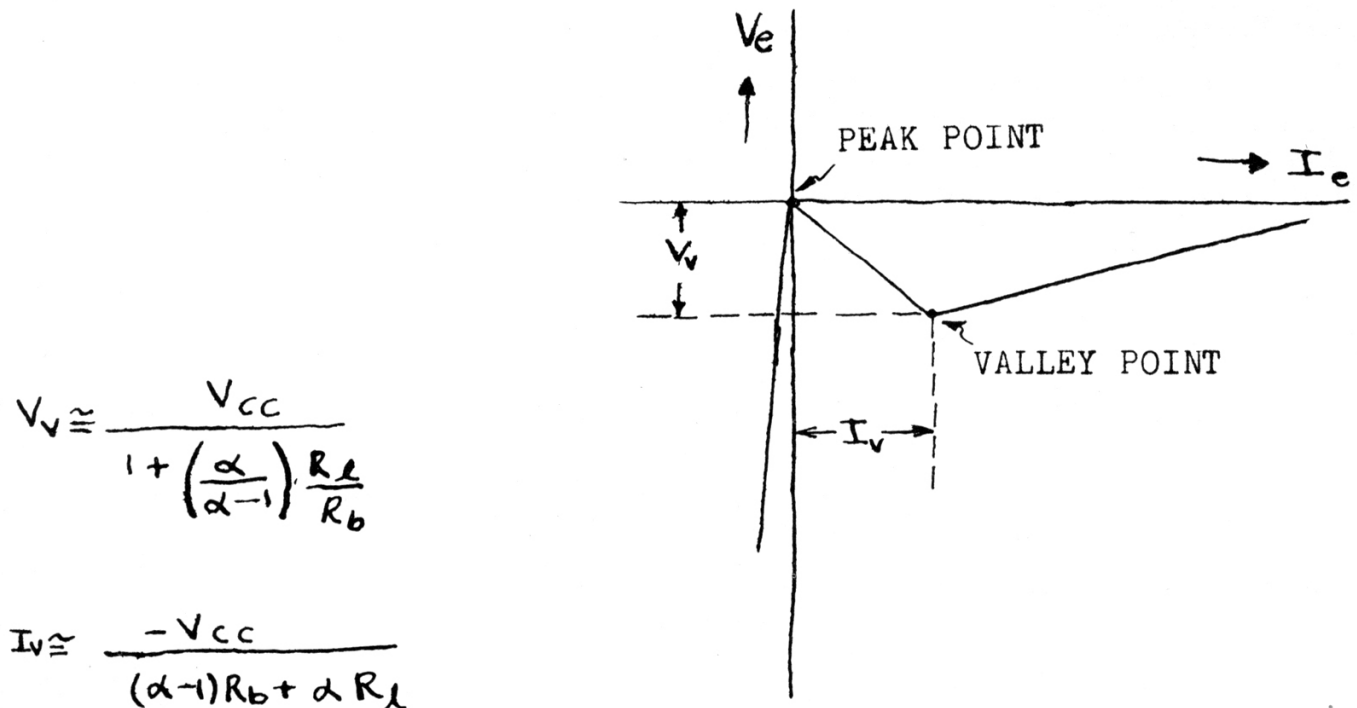
These hole storage effects are undesirable because they make the duration of the output pulse a variable, they load down the resetting signal, and if very bad they persist so long that the transistor may not be turned off by the time the base pulse has ended. Thus the circuit becomes locked up permanently in the high-current state. This is particularly serious when transformer coupling is used. The low d-c impedance of the transformer permits large average currents to flow and thereby increases the hole storage. Thus the E_3 defined previously may be much lower than E_2 . In some cases E_2 may be lower than E_1 . As a result, at the present time transformer coupling cannot be used with more than a few transistors. (Transformer coupling is desirable because it permits the major part of the signal power to be used in the load rather than dissipated in the collector resistor (R_4 of Figure 5).)

For successful use it is expected that in the circuit of Figure 5, that E_1 , defined as above, will be below -2 volts, that E_2 will be above -1/4 volt and E_3 be above -0.4 volt. This gives good margins in the circuit when X_2 is biased at -1 volt. It is found that units work satisfactorily and interchangeably, if E_1 , E_2 and E_3 are as stated above. A source of dissatisfaction is that it has not been possible to correlate the values of E_1 , E_2 and E_3 measured in the circuit of Figure 5 with the values that d-c measurements indicate. The writer feels that what is needed is more knowledge about transistor parameters in the megacycle region and more knowledge about how such parameters will affect the negative resistance. It should be emphasized that not only must more be known about transistors but more must be known about negative resistance devices when operated at frequencies where transit time considerations and storage phenomena must be considered.

5.7 CONCLUSIONS

A transistor amplifier circuit can be made to work well in high-speed switching and computing circuits. It is believed that such a transistor circuit can be used advantageously to replace many vacuum tube circuits.

IDEALIZED INPUT CHARACTERISTIC



$$\alpha = \frac{R_m + R_b}{R_c + R_b} = \left[\frac{i_c}{i_e} \right]_{R_L=0}$$

FIGURE 1

EMITTER CHARACTERISTIC

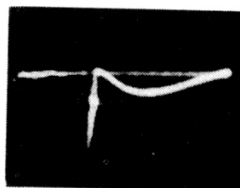
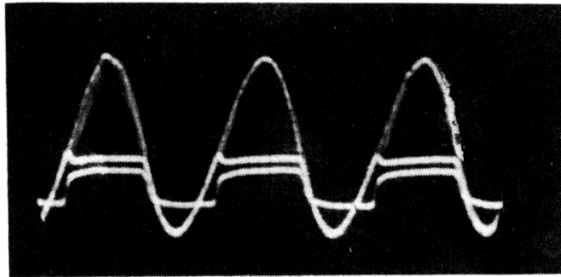


FIGURE 2

TEST CIRCUIT FOR PULSE α



WAVEFORMS WITH DA498

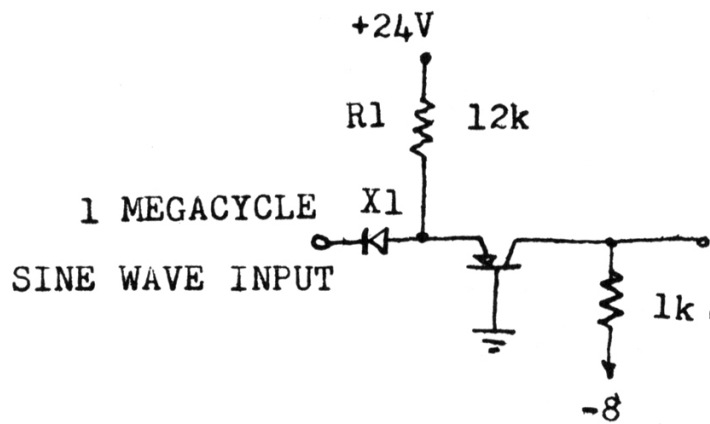
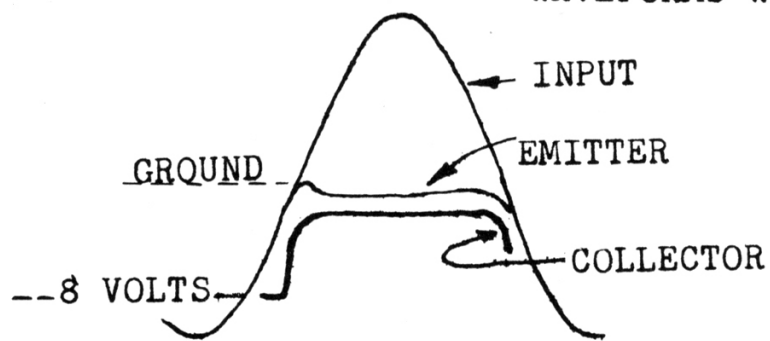


FIGURE 3

BASIC AMPLIFIER CIRCUIT

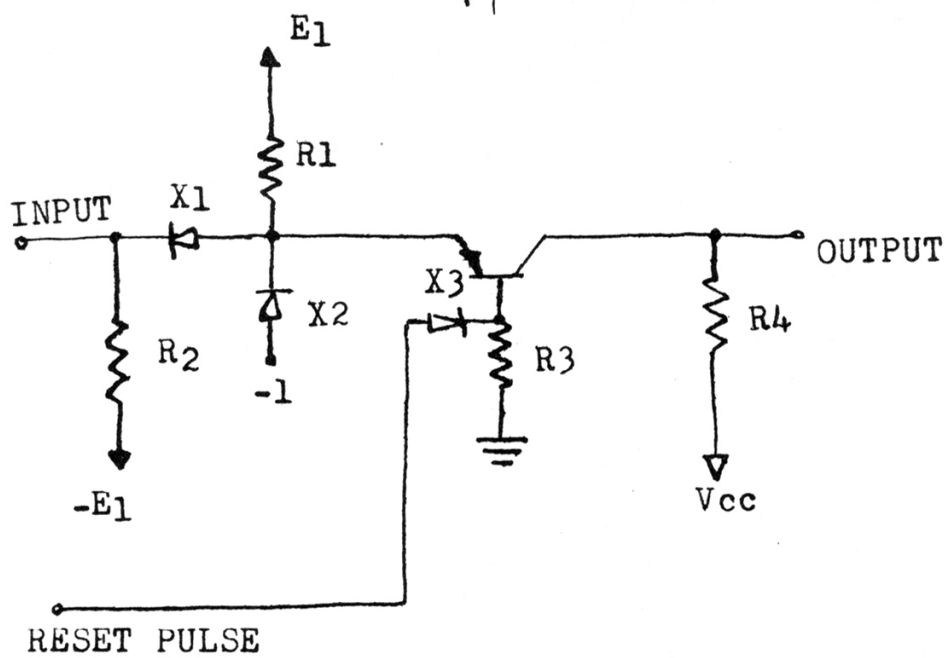
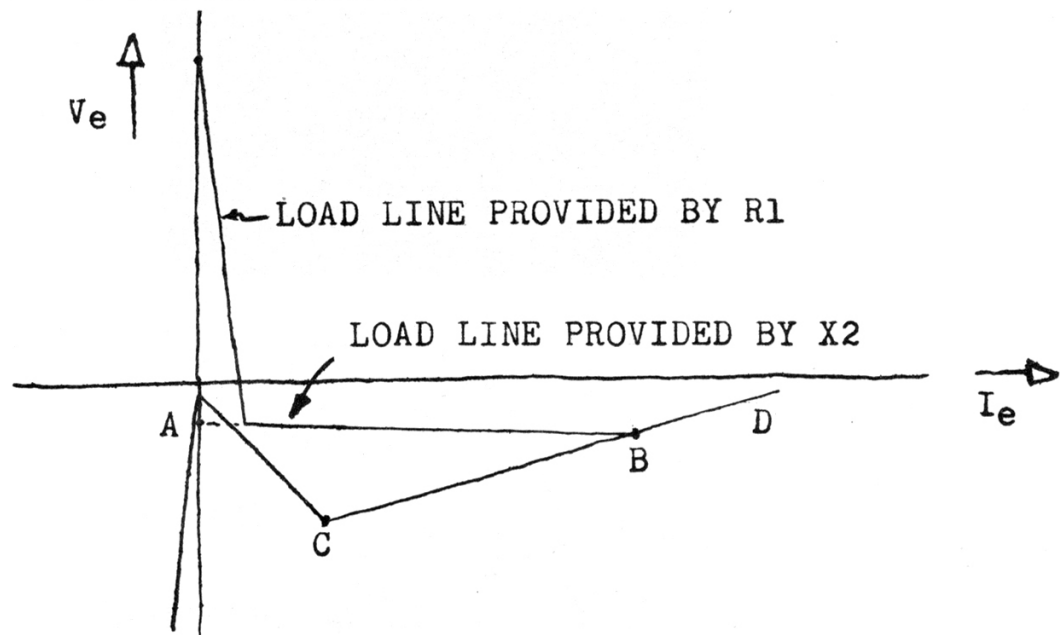
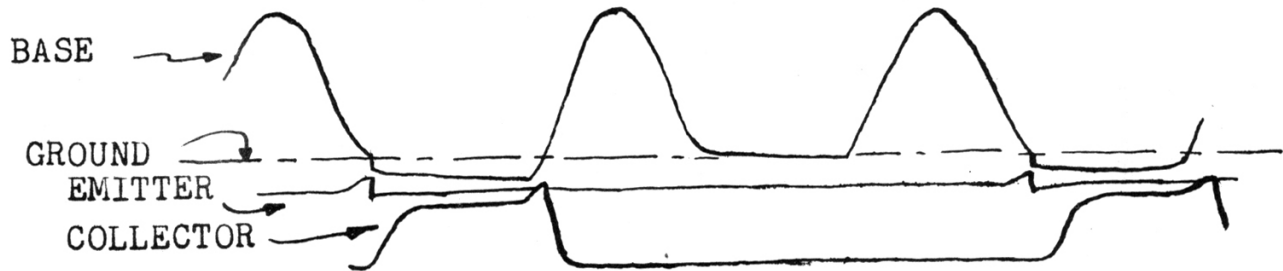
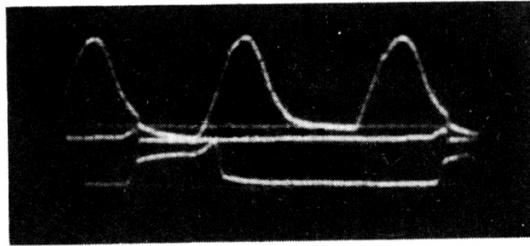


FIGURE 4

AMPLIFIER WITH WAVEFORMS



WAVEFORMS WITH DA498

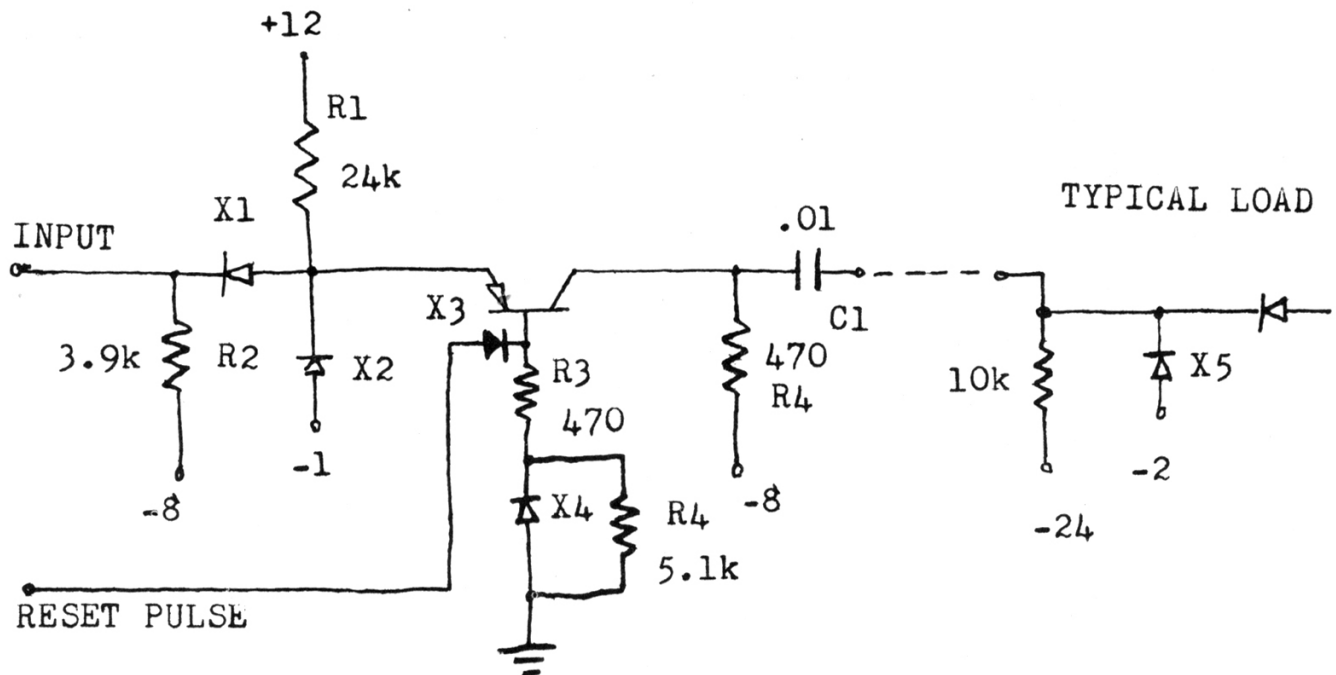


FIGURE 5

SOME ELEMENTARY 3-TERMINAL LOGIC CIRCUITS

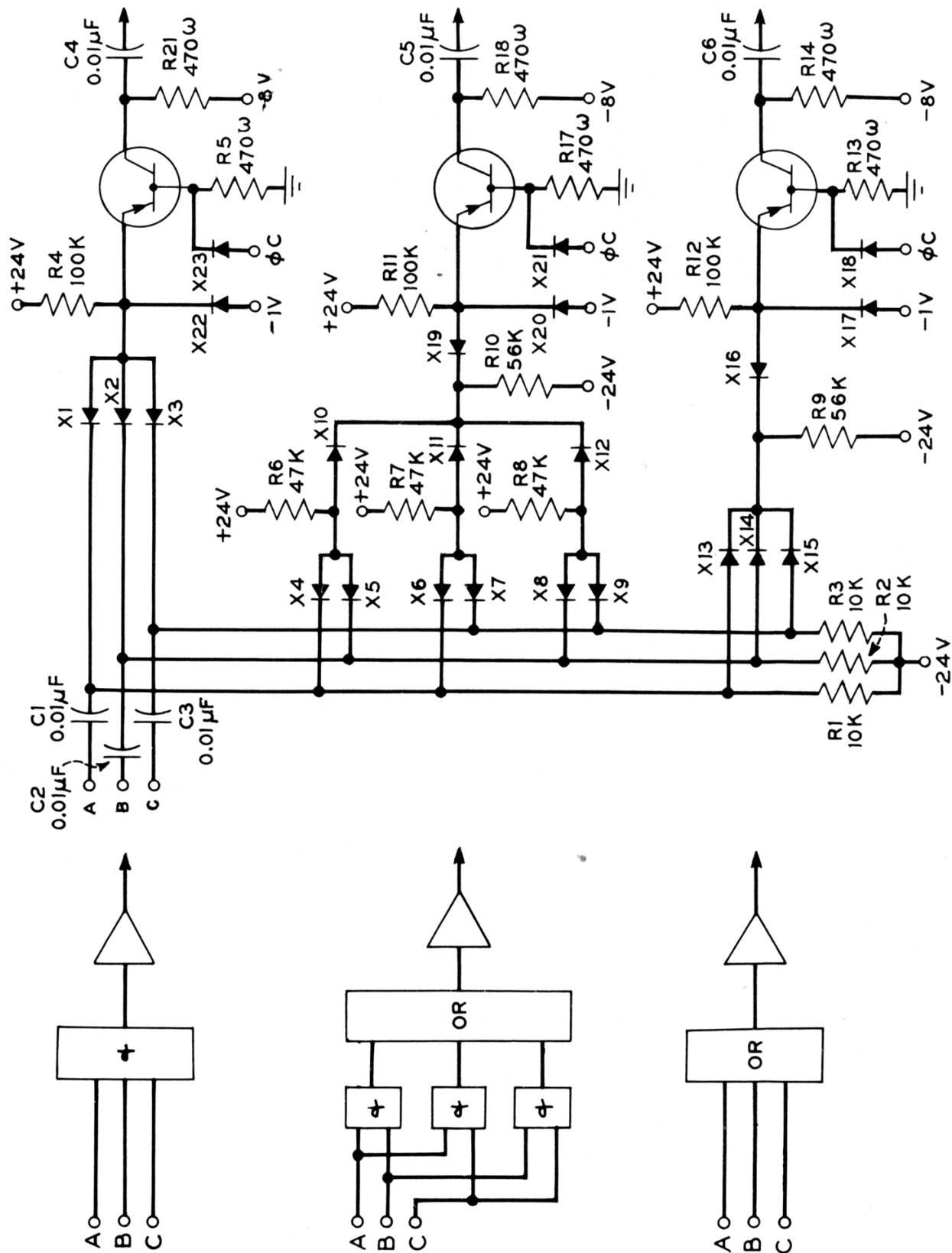


FIG. 6

INPUTS AND OUTPUTS OF 3-TERMINAL LOGIC CIRCUITS

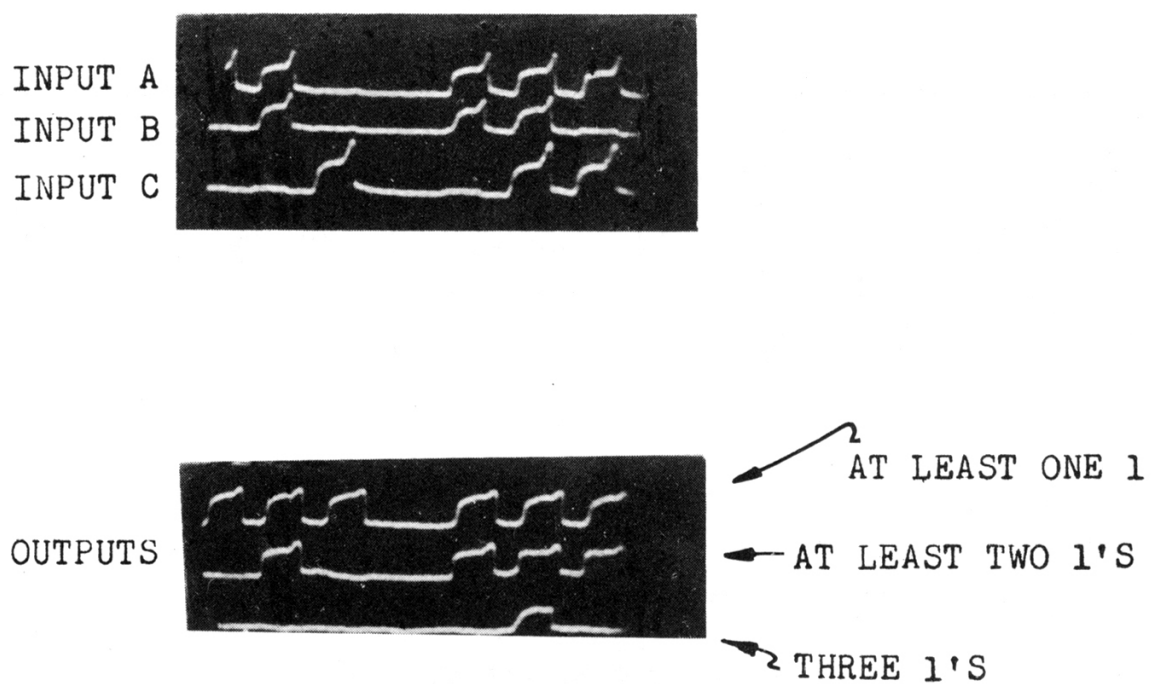
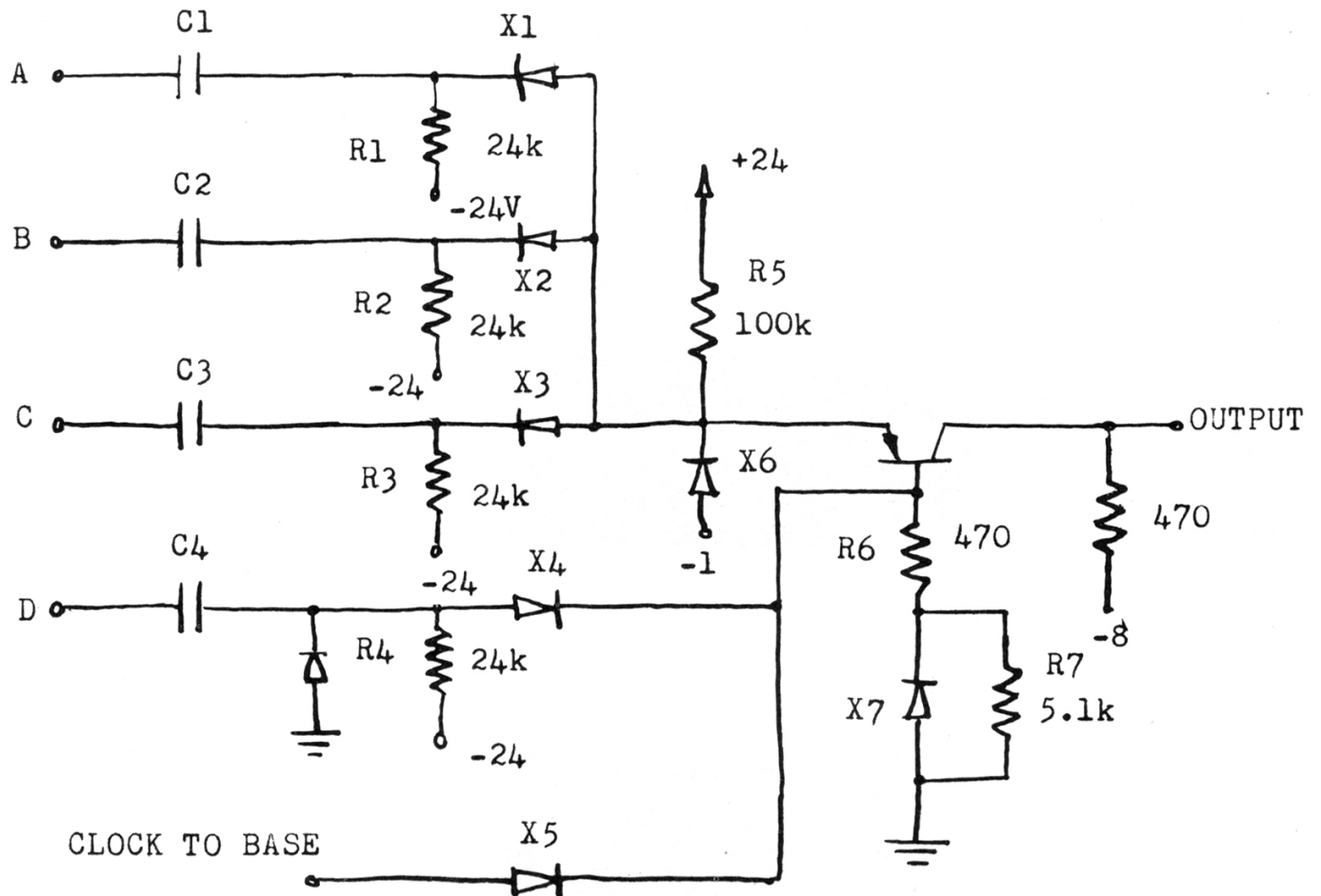
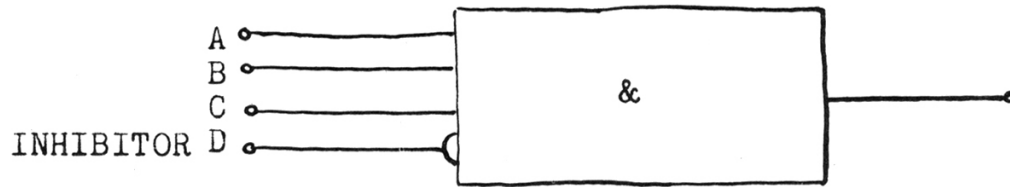


FIGURE 7

3-TERMINAL AND-CIRCUIT WITH INHIBITION



A & B SUPERIMPOSED
 INPUT C
 WAVEFORM AT EMITTER
 WITH TRANSISTOR REMOVED)
 INPUT D
 OUTPUT
 BASE WAVEFORM

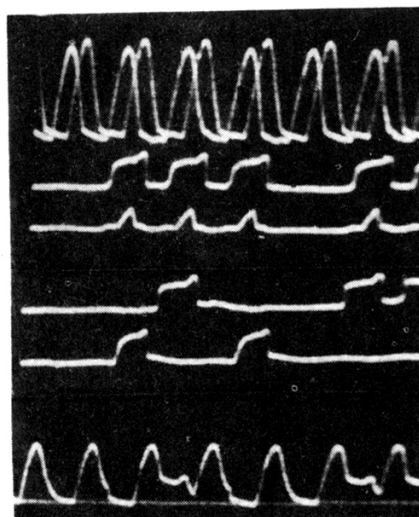


FIGURE 8

A WORD GENERATOR

6.1 INTRODUCTION

When digital computers or switching systems are developed, a fundamental device needed is a generator of numbers or words* to be used in testing the operation of the system. The device described herein generates 16 digit serial numbers in which each digit is represented by a $1/2$ microsecond pulse. The generator can be set by means of manually operated switches to generate simultaneously any 4 numbers between 0 and $2^{16}-1$. Other uses of the generator are discussed below. A front view of the word generator is shown on photograph 191565 while a back view is shown in photograph 191567.

6.2 BLOCK DIAGRAM

The generator generates the desired numbers every 16 microseconds. It is kept in rigid synchronism with the output of a 1 megacycle clock oscillator. The word pulse that constitutes the input to the unit is obtained from the megacycle clock by means of a transistor blocking-oscillator frequency divider which puts out a pulse every 16 microseconds. In the word generator this word pulse is regenerated 16 times and delayed by one microsecond 15 times (see Figure 1). The pulse appears at the output of amplifier one at zero time and represents 2^0 . It appears at the output of amplifier 16 at time 15 and represents 2^{15} . In addition to feeding a delay line each amplifier feeds one of the vertical busses shown in Figure 1 and photograph 191567. A group of 4 horizontal busses are shown in Figure 1 and each horizontal bus may be connected to any of the desired vertical busses by a manually operated switch with a diode in series to give isolation between the vertical busses (photograph 191567). At the end of each horizontal bus there is an output amplifier. The user operates the bank of 64 switches to generate the specific code groups he wants. The generated words will be available at the output amplifiers at a level suitable for driving other equipment.

- - - - -

*This device is called a word-generator in keeping with the nomenclature common in the digital-computer field. It might as well be called a number-generator or a code-group generator.

6.3 CIRCUIT DIAGRAM

Each of the twenty amplifiers shown in Figure 1 is exactly like all the others. The type was described by the author in paragraph 5. The circuit of two of the amplifiers, showing the delay line between them is given in Figure 2 which represents two successive stages in the chain of amplifiers through which the word pulse progresses.

The delay line used was obtained from the James Millen Company and has a nominal impedance of 1300 ohms and a delay of 1 microsecond per 20 inches. The delay line is made only 16 inches long so that the emitter of the n th stage will start to rise $3/4$ of a microsecond after the $n-1$ 'th stage "fires". One quarter microsecond later the base pulse from the clock will have fallen to ground and the n 'th circuit "fires" exactly one microsecond after the $n-1$ 'th. Thus the exact delay of the cable can vary considerably without changing the times at which the circuit operates.*

Figure 3 shows the emitter and base waveforms of one of the stages. (The positive peaks of the base waveform were lost in reproduction.) The figure also shows a typical number at the output of one of the word generator amplifiers.

Due to the compact nature of the amplifier construction, little stray capacitance is present. It has been found advisable to add 15 mmf from the emitter to ground in order to make the circuit less critical to transistors. This capacitance helps transistors with restricted band widths to switch from the low current to the high current state. It has also been found beneficial to operate the collector into about 50 mmf.

6.4 OTHER USES OF UNIT

The reader can see that the word generator has all the components required to convert serial codes to parallel codes. If instead of a word pulse, a serial number or code were fed into the first regenerative amplifier of Figure 2, after 16 microseconds the 16 vertical busses would carry the parallel representation of the code. Similarly if the 16 wires of a parallel system were connected to the vertical busses and a parallel number transmitted, the same number in

*The clock pulse fed to the emitter is not necessary since the base pulse locks each transistor with the clock. The diodes X1, X2, and resistor R1 would be omitted in any future design.

serial form would be available at the 16th amplifier. For this application, it would be desirable to place a diode between diode X6 and resistor R5 to prevent the word backing up in the amplifier chain.

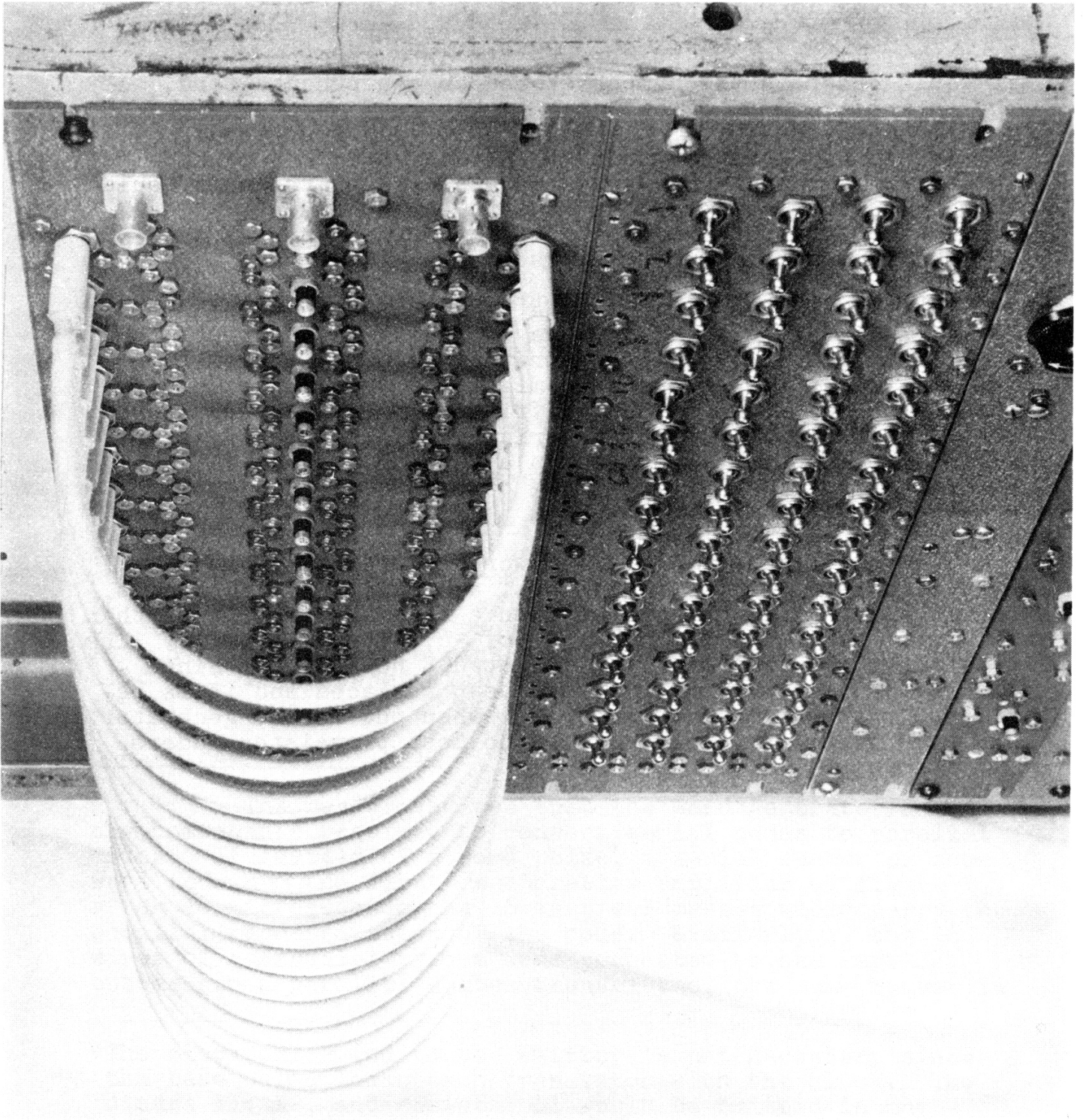
The unit might also be used to read punched cards. Consider the 16 switches connected to the top horizontal bus of Figure 2 as being feeler springs reading a punched card. If a half microsecond pulse were put into the word generator it would generate the number stored on the punched card. If the entire group of 64 switches of Figure 2 were arranged to read punched card data, the unit could read four words simultaneously. It is apparent that the switches might also be part of a commutator system on a shaft and the unit could then convert commutator positions to binary numbers. The low impedance of the transistor output circuits make such applications appear entirely practical.

Another use is for the permanent storage of numbers. If the group of 64 switches were replaced with appropriate permanent connections, the generator would always generate the same words. The generator might be extended to develop more than four words without difficulty. The numbers stored might, for example, be the numerical coefficients of some polynominal frequently needed in a computation.

6.5 CONCLUSIONS

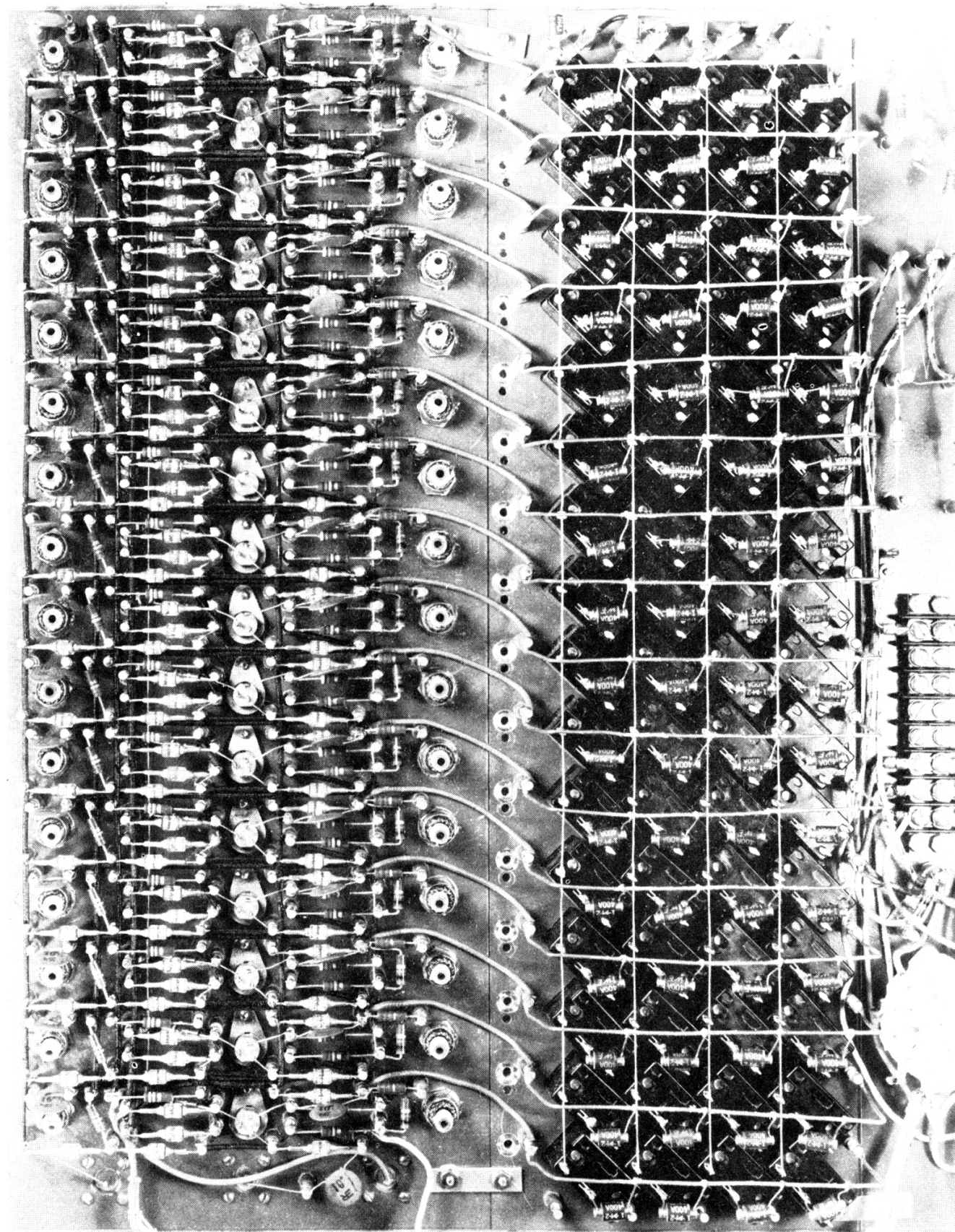
A transistor operated word-generator has been described in which 20 transistors, approximately 180 diodes, and 16 delay lines are operated on a total power of less than one watt and on battery voltages of +6, -1 and -8 volts. The unit works well and has been operated 8 hours a day since May 10, 1951. Only one unit has been replaced and it is believed that this unit was marginal when put in the generator. The word generator is being used to test transistor adders and memory units.

W O R D G E N E R A T O R



FRONT VIEW

WORD GENERATOR



REAR VIEW

The diagram illustrates a clock divider circuit with two stages, labeled N 'TH STAGE and $N+1$ 'TH STAGE. The N 'TH STAGE is the primary stage, and the $N+1$ 'TH STAGE is a subsequent stage.

Inputs:

- CLOCK PULSE:** Connected to the input of the N 'TH STAGE.
- BASE CLOCK PULSE:** Connected to the input of the $N+1$ 'TH STAGE.

Components and Connections in the N 'TH STAGE:

- Transistor:** A common-emitter transistor circuit.
- Diodes:**
 - $X1, X2$: Input diodes connected to the CLOCK PULSE.
 - $X3$: A diode connected to the base of the transistor.
 - $X4, X5, X6$: Output diodes connected to the collector of the transistor.
- Resistors:**
 - $R1$ (16k): Connected to the base of the transistor.
 - $R2$ (16k): Connected to the base of the transistor.
 - $R3$ (24k): Connected to the collector of the transistor.
 - $R4$ (470): Connected to the collector of the transistor.
 - $R5$ (2000): Connected to the collector of the transistor.
 - $R6$: Connected to the collector of the transistor.
- Capacitors:**
 - $C1$ (0.01): Connected to the base of the transistor.
 - $C2$ (15): Connected to the base of the transistor.
 - $C3$ (50): Connected to the collector of the transistor.
- Delay Line (DL):** A 3/4 MICRO-SECOND DELAY line connected to the collector of the transistor.

Outputs:

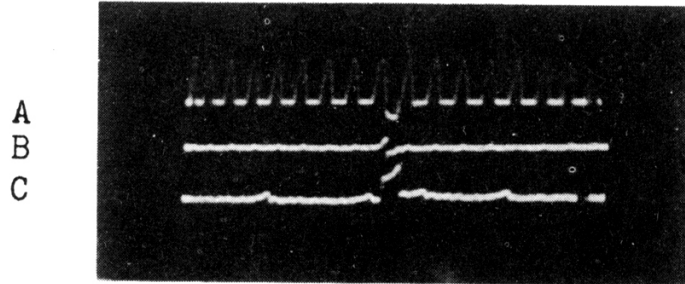
- PULSE AT N :** The output of the N 'TH STAGE.
- PULSE AT $N+1$:** The output of the $N+1$ 'TH STAGE.

Other Labels:

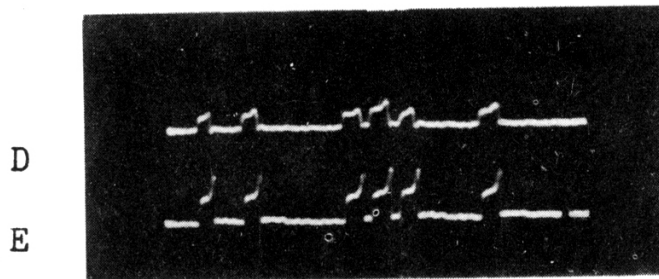
- FROM PRECEDING STAGE:** A label indicating the input to the N 'TH STAGE.
- 6, -8, -1:** Numerical values associated with the output signals.

- 725 -

WAVEFORMS IN WORD GENERATOR



- A. BASE WAVEFORM AT 10 TH STAGE
- B. EMITTER WAVEFORM AT 10 TH STAGE
- C. COLLECTOR " " " "



00101000 111 001 DECIMAL 10,004

- D. TYPICAL NUMBER OUT OF DIODE MATRIX
- E. NUMBER AFTER REGENERATION

FIGURE 3

DESIGN OF HIGH SPEED DIGITAL COMPUTERS USING TRANSISTORS

DELAY LINE STORAGE

7.1 INTRODUCTION

In section II, the writer described a method of building a digital computer based on a transistor amplifier, diode logic circuits, and electric delay line storage. In section V, the basic transistor amplifier was described together with the basic diode circuits. In this memorandum the work is continued with the description of a delay line storage cell (Figures 1 and 2) which will store 16 digit numbers at the price of only three active elements. Photographs 191566 and 191568 show front and back views of two storage units now in use.

7.2 DELAY LINE

The delay cable used was made by the James Millen Company and has a delay of about one microsecond per twenty inches. It is not the voltage attenuation of the line that requires the use of three amplifiers in the device pictured but is the time distortion suffered by a half-microsecond pulse after 5 microseconds delay. With a lumped-parameter delay line of greater bandwidth it is believed that a 16 digit word could be stored with only one regenerating amplifier.

7.3 CIRCUIT DIAGRAM

The complete diagram of the unit is shown in Figure 1. The transistor amplifiers have been described in detail in paragraph 5. It may be noted that the amplifier is turned on primarily by the signal from the preceding delay line but it cannot be turned on until the clock pulse at the base has fallen to ground and it will be turned off when the clock pulse rises one-half microsecond later. Each delay line is made $1/4$ microsecond shorter than the total delay desired so that the output pulse will have been at the emitter one-quarter of a microsecond before the clock pulse at the base has fallen to ground. This arrangement permits the delay lines to vary in delay and rise time without upsetting the synchronism imposed by the clock.

The switch S1 is used to empty the delay line by inhibiting the first transistor. In a full-fledged computer application S1 would be removed and an inhibiting circuit would be placed at the output of DL3. Whenever a new word is to be stored, the inhibitor circuit would be pulsed and prevent the old word from circulating any longer.

The output of delay line 3, and the emitter, base and collector waveforms of the transistor it feeds are shown on Figure 2. The word being stored was developed by the word generator described in paragraph 6.

7.4 CONCLUSIONS

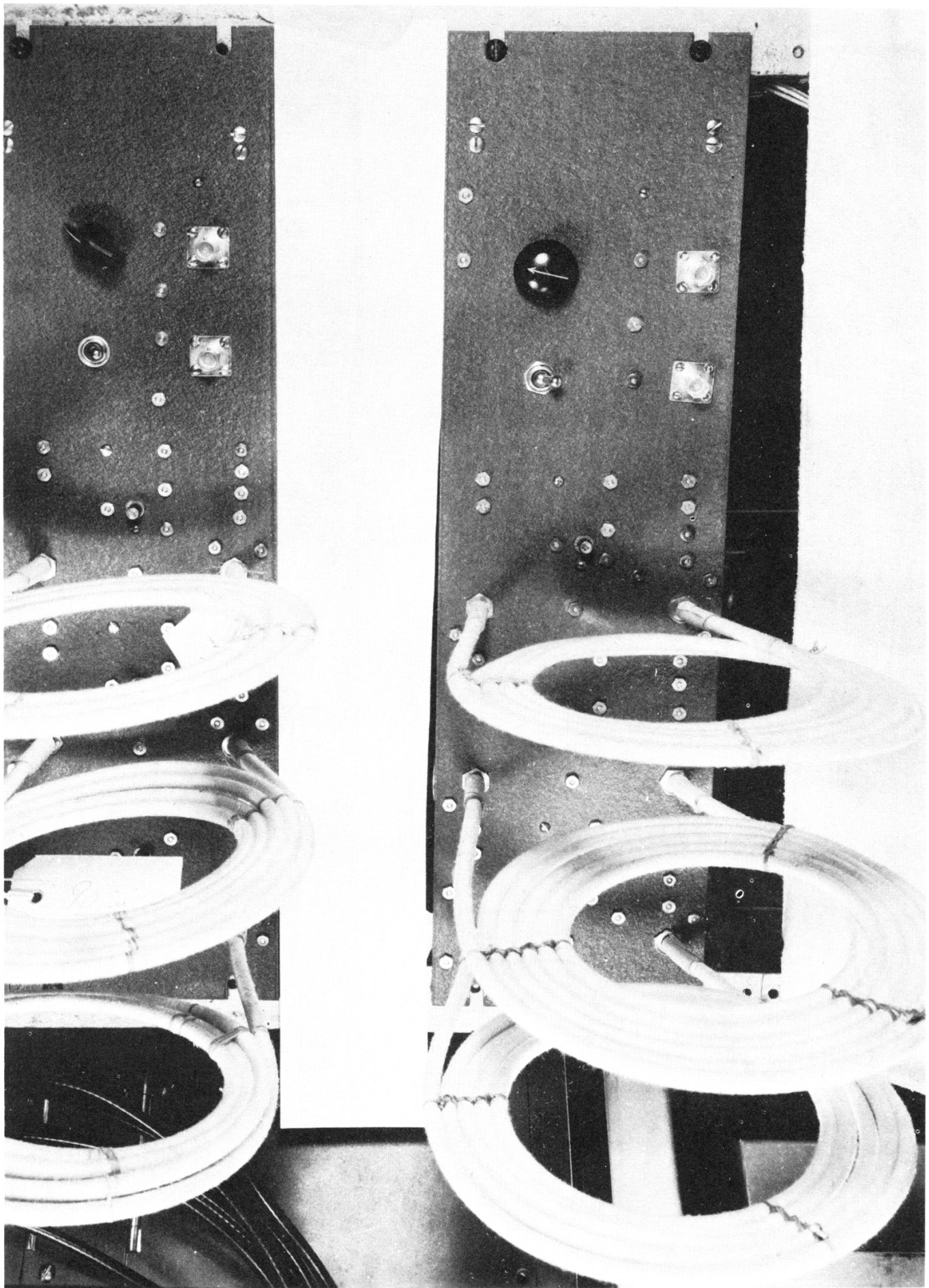
A 16 digit delay line storage device has been described which offers a more efficient storage facility than flip-flop or shift-register storage. It has another advantage in that it can be emptied of stored data by turning off one transistor rather than 16. This is very important where hole storage effects make it difficult to turn off more than one transistor with the output of another transistor.

The device has been operated 8 hours a day for over a month (since its construction) without transistor replacements. The unit makes a convenient device for the testing of transistors for random errors since if a word is introduced into the unit just once and then left to circulate, one transistor error will mutilate the word permanently.* It has been possible to operate the unit for over 48 hours without failure.

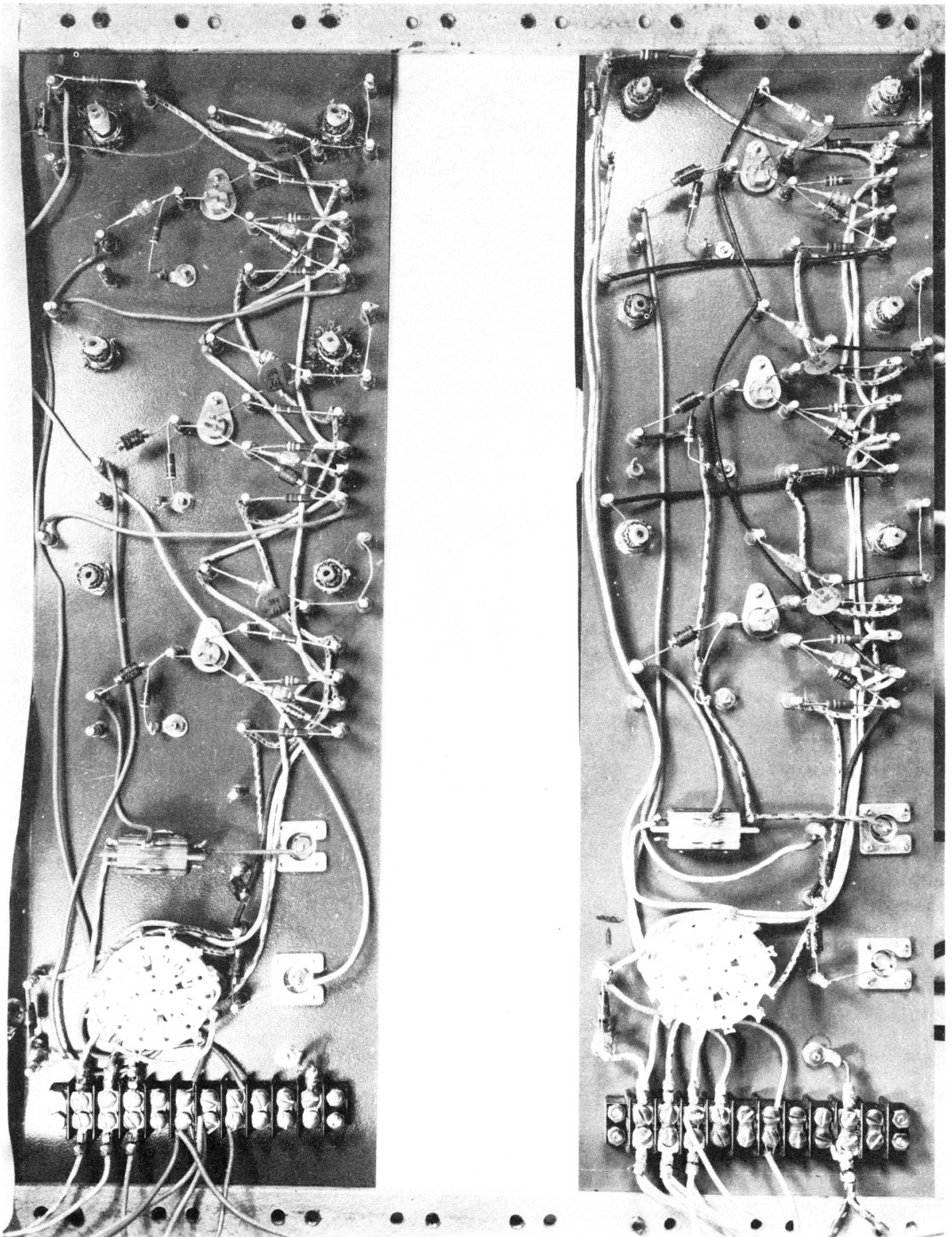
This is the equivalent of 500 billion successful transistor discriminations. When a megacycle clock is available which will operate in spite of a-c power shutdowns, it is hoped that long term tests can be run.

*Transistors produced for digital applications might profitably be "aged" in such a circuit before they are delivered to a prospective user.

DELAY LINE STORAGE UNIT



DELAY LINE STORAGE UNIT



REAR VIEW

DELAY LINE STORAGE

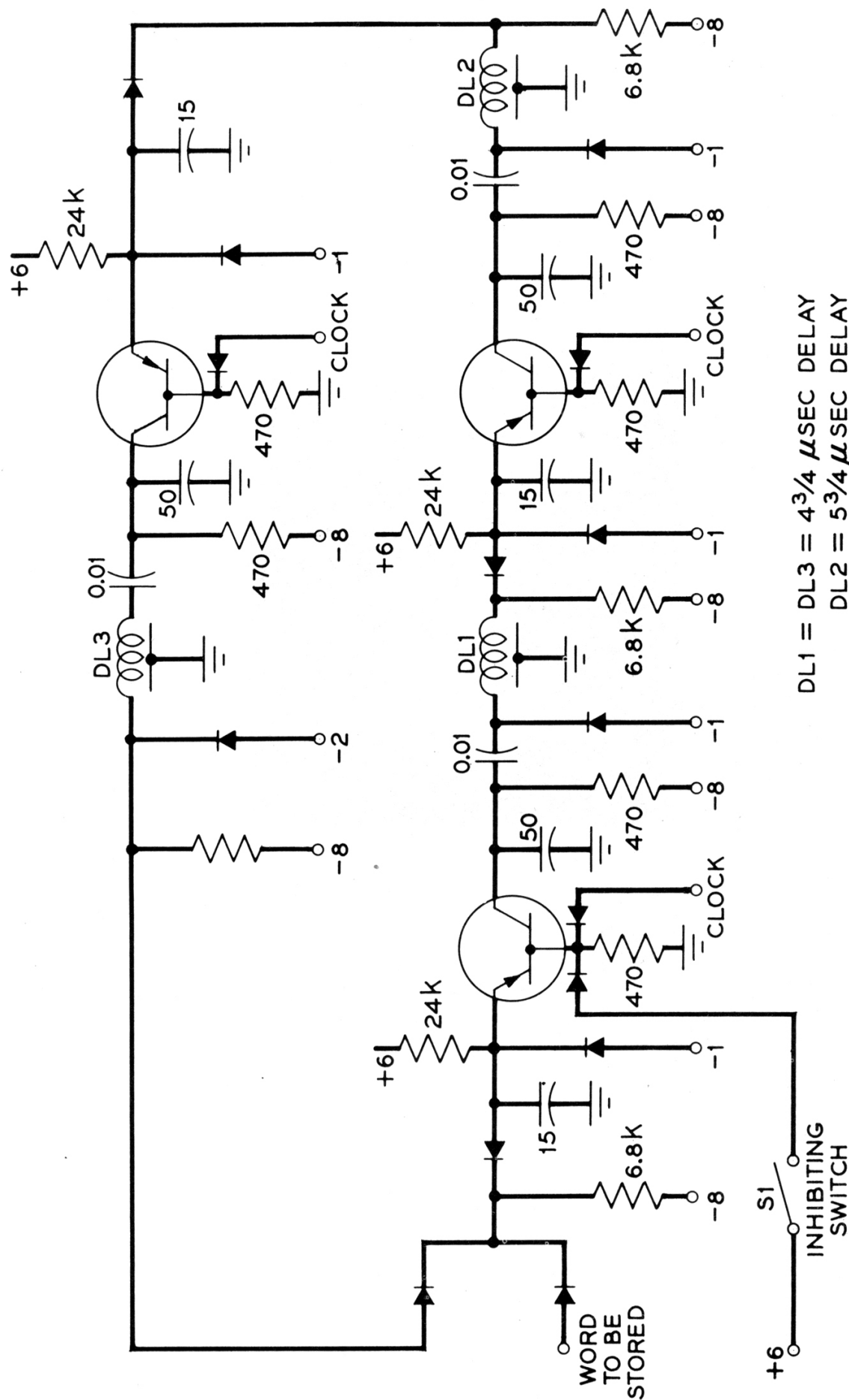
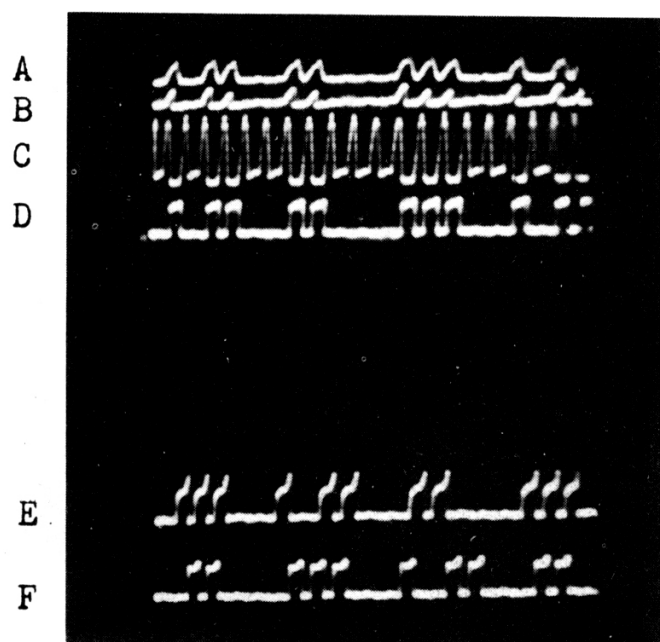


FIG. 1

WAVEFORMS IN STORAGE UNIT



- A - OUTPUT OF DL3
- B - EMITTER OF FIRST STAGE
- C - BASE OF FIRST STAGE
- D - COLLECTOR OF FIRST STAGE
- E - COLLECTOR OF SECOND STAGE
- F - COLLECTOR OF THIRD STAGE

FIGURE 2

BIT STORAGE WITHOUT FLIP-FLOPS

8.1 INTRODUCTION

Many of the storage requirements of a serial computer can be met by delay line storage in which a word to be stored is re-circulated in a one word delay line and kept in synchronism with the rest of the computer by means of regenerative amplifiers. This type of storage is quite efficient since for example, 16 digits can be stored with the use of only three transistors as regenerative amplifiers. A mechanization of this type of storage was described by the author in paragraph 7 above. Even in serial computers, however, this form of storage cannot be used for all storage functions. There are some places in a computer where the stored information has to be continuously available and cannot be available only once every word period. For example, there are places in a computer where switches are required. These switches normally must be self locking; that is, when a switch has been closed it is supposed to remain closed until it receives an instruction to open. When it is opened, it must remain open until it receives an instruction to close. There must be some memory element associated with the switch which stores the close instruction or stores the open instruction and keeps the switch in the desired state. It has been customary to use flip-flops for this type of storage.

This memorandum describes a different storage circuit for such use. It is called a bit storage cell because it can store one binary bit of information, either a 1 or a 0. In Figure 1, the schematic representation of the circuit is shown as a box with a M standing for memory, with an output terminal, and 2 input terminals: one input terminal is labeled "one" and the other labeled "zero". This device has the property that if a pulse is put on the one terminal, a 1 will be regenerated continuously at the output until a pulse is put on the zero terminal, in which case the output will be 0 and remain 0 indefinitely unless a new pulse is put on the one terminal. Thus it is seen that the output of this device is a train of pulses occurring at the clock frequency when a 1 is stored and when a 0 is stored there is no output at all.

A typical use for this type of storage is also shown in Figure 1 where the mechanization of a single pole switch is given. The memory circuit feeds one terminal of an and-circuit which has its other terminal connected to the signal to be switched. If a pulse is fed to the one terminal of the memory circuit, the switch will be closed and whatever data is put on the input to the switch will appear on the output. If on the other hand, a pulse is put on the zero terminal of the memory circuit, the memory circuit will have no output thereafter and the switch will be open because the and-circuit cannot respond to the input on the in terminal.

8.2 POSSIBLE MECHANIZATIONS

A mechanization for this type of storage is shown in Figure 2A. If a pulse is put on the one terminal of the device, it will go into the amplifier through the or-circuit and the inhibitor-circuit and will appear as an amplified pulse at the output of the amplifier. This pulse will travel back through the one digit delay line into the amplifier and continue to recirculate indefinitely appearing once every digit period at the output of the amplifier. The inhibitor-circuit is put in series with the circulating path so that if a pulse is put on the inhibition lead it will prevent the output of the delay line from getting back into the amplifier. This scheme is not considered very efficient because it requires a 1 digit delay line and if this is made out of the delay line materials now available, it will be a very bulky component. Since it is only necessary that 1 digit be delayed by 1 digit time in order to implement this device, a delay line isn't really required. Suppose that the output pulse of the amplifier, which is normally a positive pulse, is inverted to be made a negative going pulse and this negative going pulse is put across a parallel tuned circuit. The output pulse will cause the parallel circuit to ring negative and then after a delay ring positive. This positive ring can be fed back into the or-circuit, of Figure 2, to retrigger the amplifier. To implement this scheme it is necessary to have a transformer, to convert the positive going amplifier output to a negative pulse, and a resonant circuit. A little thought reveals that the resonant circuit can be combined with the transformer since the transformer that inverts the pulse may itself be made to ring. This scheme is shown in Figure 2B where the transformer is fed through a series resistance.

The series resistor in effect decouples the transformer from the amplifier and prevents the low output impedance of the amplifier from damping the transformer. This makes it a poor transformer but a good ringing device. It also prevents the transformer from loading down the amplifier appreciably.

8.3 CIRCUIT DIAGRAM

In Figure 3 a specific circuit is shown. The amplifier used was described in paragraph 5 above. When a 1 is put into the one terminal of the memory circuit it fires the transistor which causes the collector to go positive. The clock pulse at the base turns the transistor off $1/2$ microsecond later. The pulse at the collector passes current into transformer T2 through R5 and causes the transformer inductance together with the shunt capacity presented by the circuit to ring. After the pulse at the collector has disappeared the transformer secondary rings positive and through diode X6 retriggers the transistor provided that an inhibitor pulse has not been fed to transformer T1. The clock pulse at the base of the transistor insures that the transistor will not fire until the preceding digit period is finished. An inhibitor pulse fed to T1 will be inverted and through diode X2 will hold the emitter negative thereby preventing a stored pulse from recirculating.

The two transformers T1 and T2 are miniature transformers designed by Mr. A. H. Bobeck. These transformers are designed to pass a $1/2$ microsecond pulse into a 470 ohm load. When operated from a high impedance generator and into a light load, these transformers ring at about one megacycle in response to a step pulse.

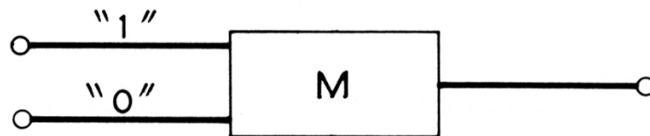
Figure 4 shows typical wave forms in a memory circuit. The input pulses applied to the one terminal and the zero terminal of the memory device are taken from the word generator described in paragraph 6. A 1 is stored in the memory device at time one. Four microseconds later, a pulse is put on the zero terminal and empties the storage cell. At time 6 another pulse appears on terminal one but does not get through the amplifier because at the same time a pulse is received on the zero terminal. The pulse at time 7 goes through the amplifier, but it does not recirculate because at time 8 a pulse is put on the zero lead. The output of the device is 0 until time 11 when another pulse appears on the one terminal. This pulse is stored for 4 digit periods until another pulse is put on the zero terminal and empties the cell.

Since the regenerative amplifier used in this device is itself a bi-stable device and is only made to look like an amplifier by being turned off every digit time by a clock pulse, the reader may ask why isn't the bi-stable transistor circuit used for memory. The reasons are as follows: The bi-stable transistor circuit can be turned on quite easily since the emitter represents a high impedance when the transistor is in the low current state. However, once the transistor is locked up in the high current state, both the emitter and base terminals present very low impedances and it takes considerable current to shut off the device. In the computing schemes the writer has proposed it is never necessary to turn off one transistor by another. Transistors are used only to turn on one another and the shut-off pulses are developed from a clock. Since the clock signal represents steady state power, it is felt that it can be generated efficiently. If the bi-stable transistor circuit were used for a memory circuit it would be left locked up in its high current state until it was desired to store a 0 and a transistor some place in the computer would have to develop enough current to shut off the transistor at that time. In the scheme shown in Figure 3, it is no more difficult to store a zero than a one, because the storage of a zero merely requires that a positive pulse be applied to T1. T1 converts the pulse to a negative going pulse, which causes diode X4 to conduct. It is only necessary for diode X4 to carry slightly more than a quarter of a milliampere to prevent the transistor circuit from firing. The merit of the circuit can be seen, therefore, to lie in the fact that it can be made to store a 1 or a 0 equally well and the sensitivity to a change in either direction is the same.

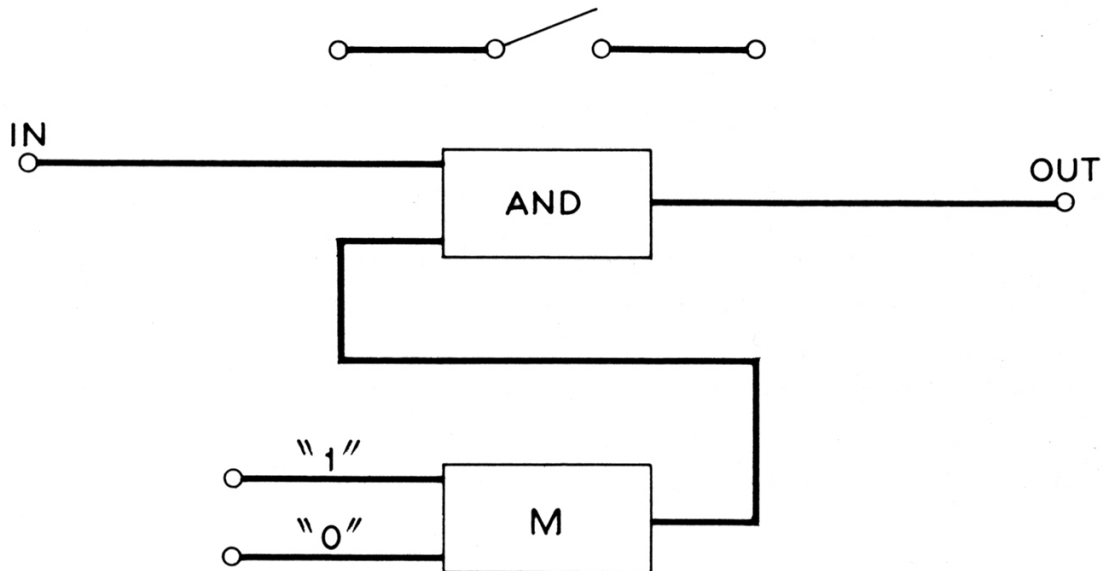
8.4 USE OF CIRCUIT FOR DELAY

The device described herein makes a useful delay element where only one digit of delay is required. In Figure 5 a chain of amplifiers are shown which are connected to one another through ringing transformers. If an input pulse is put into amplifier one, it will appear at amplifier two at time 2, amplifier three at time 3, etc. The circuit might be an important substitute for delay lines where long delays are required and delay lines themselves might be too bulky.

BIT STORAGE CELL
SYMBOLIC REPRESENTATION AND TYPICAL USE



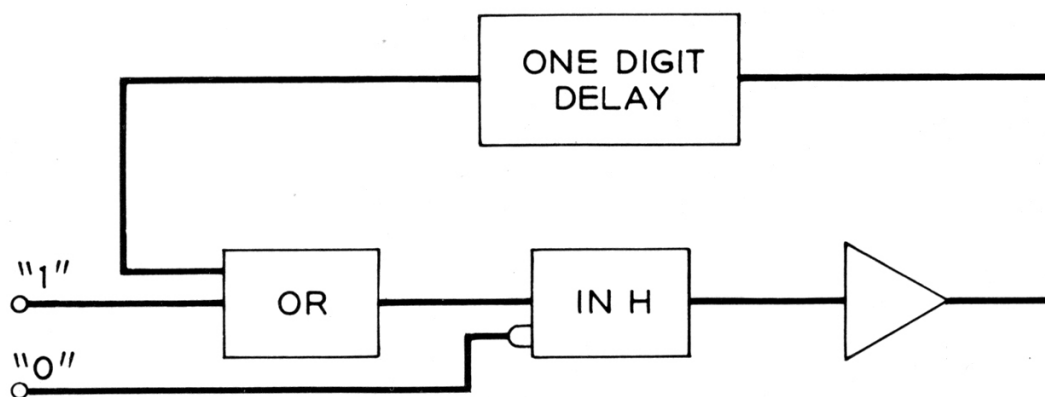
(a) SYMBOLIC REPRESENTATION



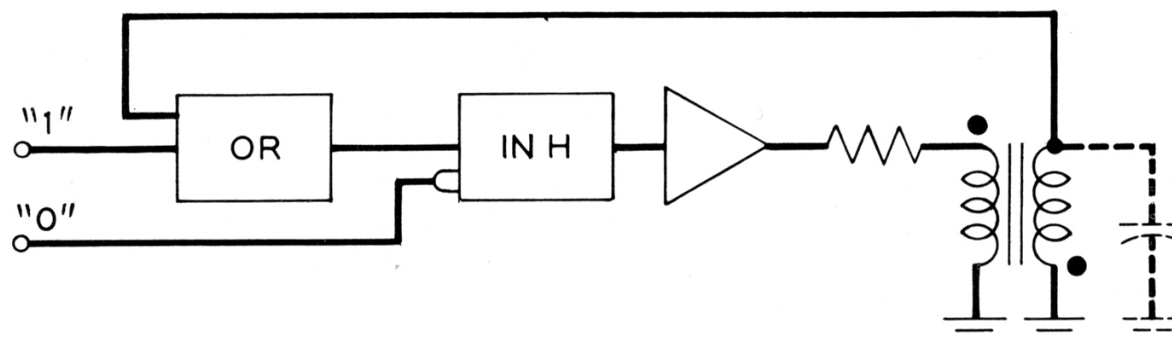
(b) SINGLE-POLE SWITCH

FIG. 1

BIT STORAGE CELL POSSIBLE MECHANIZATIONS



(a) DELAY LINE STORAGE



(b) RESONANT CIRCUIT FOR DELAY

FIG. 2

CIRCUIT OF MEMORY CELL

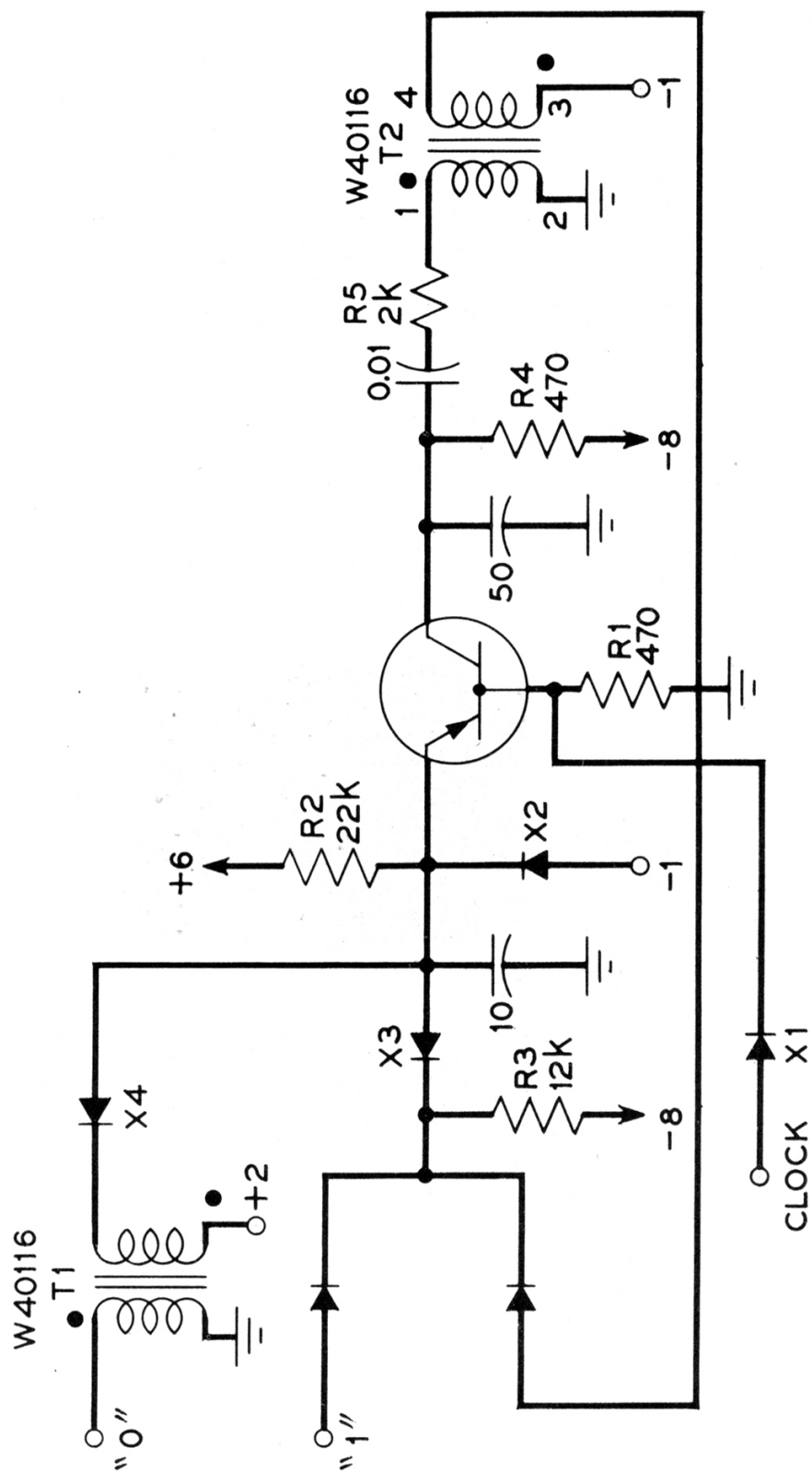


FIG. 3

WAVEFORMS IN STORAGE CELL

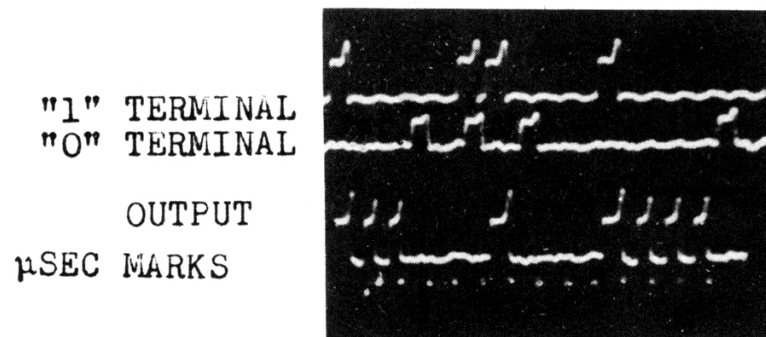
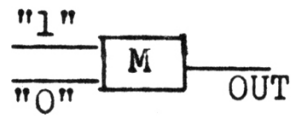


FIGURE 4

BIT STORAGE DELAY SCHEME

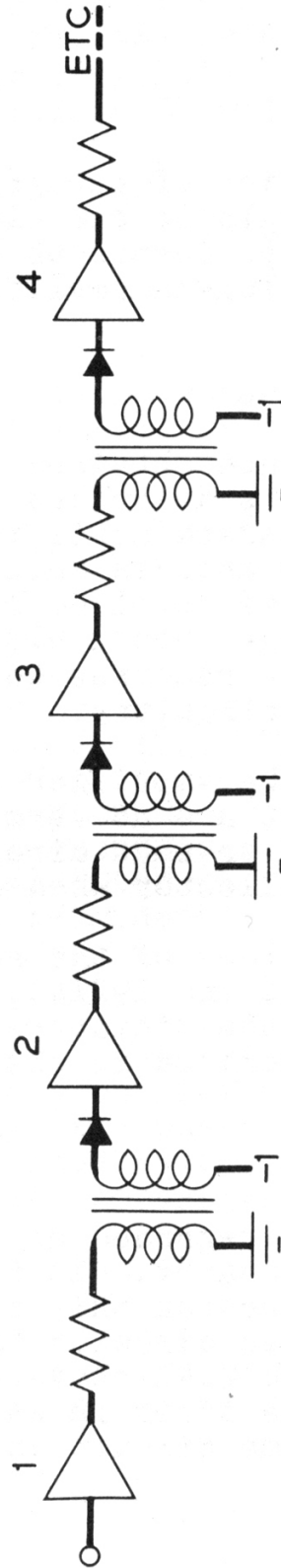


FIG. 5

A BINARY ADDER

9.1 INTRODUCTION

The basic amplifier of paragraph 5 has been combined with the appropriate diode logic circuits to produce a serial adder. The adder can accept inputs at a megacycle rate and uses six interchangeable plug-in amplifiers. The total battery drain is 0.264 watts.

9.2 BASIC AMPLIFIER PACKAGE

From the experience obtained with the word generator and delay line storage units described in preceding paragraphs it was apparent that a standard amplifier package would speed up the construction of new devices such as the adder described herein. The package that was evolved represents only a crude approximation to the package that would be used in production because time did not permit recourse to such techniques as auto-assembly and printed circuitry.

The circuit of the amplifier is shown in figure 9-1. The normal input and output are at terminals 2 and 12. Terminals 3 and 11 are provided so that direct connections can be made to the emitter and collector when desired.

Front and back views of the assembled amplifier are shown in photographs 192144 and 192143. The small cylindrical object shown in 192144 is the miniature transformer that is used for inhibition as described in the detailed discussion of the adder.

9.3 ADDER CIRCUIT

The adder can be regarded as a translator with three inputs, addend, augend and carry. It is a simple translator in that the output is a function only of the number of ones among its inputs. The logic circuits for performing addition were described in paragraph 2.41 above. Figure 9-2 shows the schematic of a complete adder in which each of the amplifiers in 9-2 has the same circuit as the one in figure 9-1.

If there is at least one "one" among the inputs either diode X9, X10, or X11 will pass current into amplifier B3 which will produce a half-microsecond output. If there is only one "one" among the inputs, 4 out of the 6 diodes X3, X4, X5, X6, X7, and X8 will not cut-off and amplifier B2 will not fire. Similarly, X1 or X2 or the internal diode X3 of amplifier B1 will continue to conduct and B1 will not fire.

If there are two ones among the inputs either X3 and X4 or X5 and X6 or X7 and X8 will be cut off which will put $3/4$ of a milliampere through X12, X13, or X14 to fire amplifier B2.

If there are three "ones" among the inputs, X1, X2, and X3 (internal to B1) will be cut off and amplifier B1 fires.

When amplifier B3 is triggered a half microsecond pulse passes current through X22 which cuts off the diode X3 internal to B5. Amplifier B5 will fire when the diode X18 is cut off by the clock provided amplifier B2 has not fired. If amplifier B2 has fired the transformer T1 will invert the positive output pulse and cause X19 to conduct which will prevent B5 from firing. The purpose of feeding the clock pulse to X18 is to insure that B5 will not fire on the input of B3 until after B2 has had an opportunity to inhibit B5. It should be recognized that B5 cannot fire until X18, X19, and the X3 internal to B5 have all been cut-off. The diode X19 will permanently be cut-off, unless B2 fires, because it is returned to +2 volts.

The output of B5 is restored to a DC level of -2 volts by diodes X20 and R8. When B5 fires it will trigger B4 through X16 to produce a one for the sum. The firing of B1 will trigger B4 through X15 whether or not B5 has operated. The carry is obtained by feeding the output of B2 through a half microsecond delay line to trigger B6.

It was explained in paragraph 5 on the basic amplifier circuit that the phase of the base pulse supplied by the clock determines when an amplifier will be able to fire. The clock used has 4 outputs, Φ_a , Φ_b , Φ_c , and Φ_d , each of which is delayed by $1/4$ microsecond from the preceding one. The inputs to the adder are obtained from amplifiers whose bases were operated on Φ_c . The amplifiers B1, B2 and B3 are

operated on Φ_d to permit the Φ_c outputs to pass through the diode circuits. This results in the outputs of B1, B2 and B3 being delayed exactly $1/4$ microsecond from the addend, augend and carry.

Amplifier B5 is operated on Φ_a to permit the outputs of B2 and B3 to rise and amplifier B4 is therefore operated on Φ_b . This results in the sum signal being delayed $3/4$ microseconds from the addend, augend and carry. Delay line one is required to delay the output of amplifier B1 by $1/4$ microsecond so it will be in phase with the output of B5.

The carry pulse has to be in phase with the addend, and augend which are Φ_c . Since $1/4$ of a microsecond is lost in both B2 and B6 delay line 2 need be only $1/2$ microsecond long.

The addend, augend, and carry inputs are obtained through capacitors (C3 of figure 9-1) and their DC level is set at a voltage below $-1 \frac{1}{2}$ volts by the internal diode X2 of amplifier B1. This diode X2 is returned to $-1 \frac{1}{2}$ volts whereas the diode X2 of each of the other amplifiers is returned to the normal value of -1 . The reason for setting the DC level of the inputs at below $-1 \frac{1}{2}$ volts is to prevent the voltage drop across diodes X3, X4, X5, X6, and X7 and X8 from raising terminal 2 of B2 above -1 volt in the absence of signals. It should be noted that R4 is made 2.7 k rather than 2.2 k because it has 12 k, R3 of amplifier B1, in parallel with it whereas R5 and R6 are not shunted.

The input signal required to operate the adder can be computed by studying the addend requirement alone since the augend requirements are the same. In the absence of a signal the junction of R5 and X1 rides at a voltage below $-1 \frac{1}{2}$ volts determined by the drop across diode X1. Assuming that the drop across X1 is about $1/2$ volt the current through R5 can be calculated as

$$\frac{8 - 2}{2.2}$$

or 2.73 milliamperes. The drop across X1 (a W.E. 400A varistor) for a 3 milliamper current will average $1/2$ volt and this checks that the addend terminal will ride at -2

volts in the absence of a signal. To insure that the emitters of B1, B2 and B3 can be carried above their turning point (assumed to be no higher than ground) the addend terminal has to be carried to about +0.25 volts. The current required to do this is

$$\frac{8 + 0.25}{2.2}$$

or 3.75 milliamperes. The voltage change required is 2.25 volts. The input requirement on the adder is therefore a 2.25 volt pulse and a current of 3.75 milliamperes.

If the diodes available has been ideal (zero forward impedance) the input voltage would have been only 1 volt and the current only 2/3 of a milliampere. In this case if the peak point of transistors could be held to a spread of 0.25 volts the input requirement to the adder could be only 0.25 volt. It is hoped that the above discussion indicates how the forward impedance of diodes and the dispersion in transistor peak points affect signal power required.

Figure 9-3 shows the wave forms at various points in the adder for the addition of two typical numbers. Photograph 192399 shows a front and back view of the adder. Photograph 192400 shows a front and back view of the diode package designed for the logic circuits at the front end of the adder.

9.4 SUMMARY

A successful all transistor high speed adder has been described. This is the third such adder that the writer has built. The first two have been operating since May 1951 without any transistor replacements.

PACKAGED AMPLIFIER

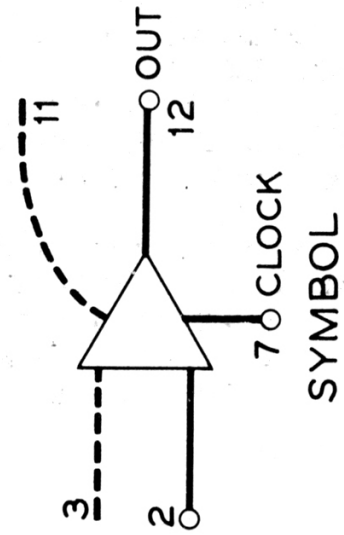
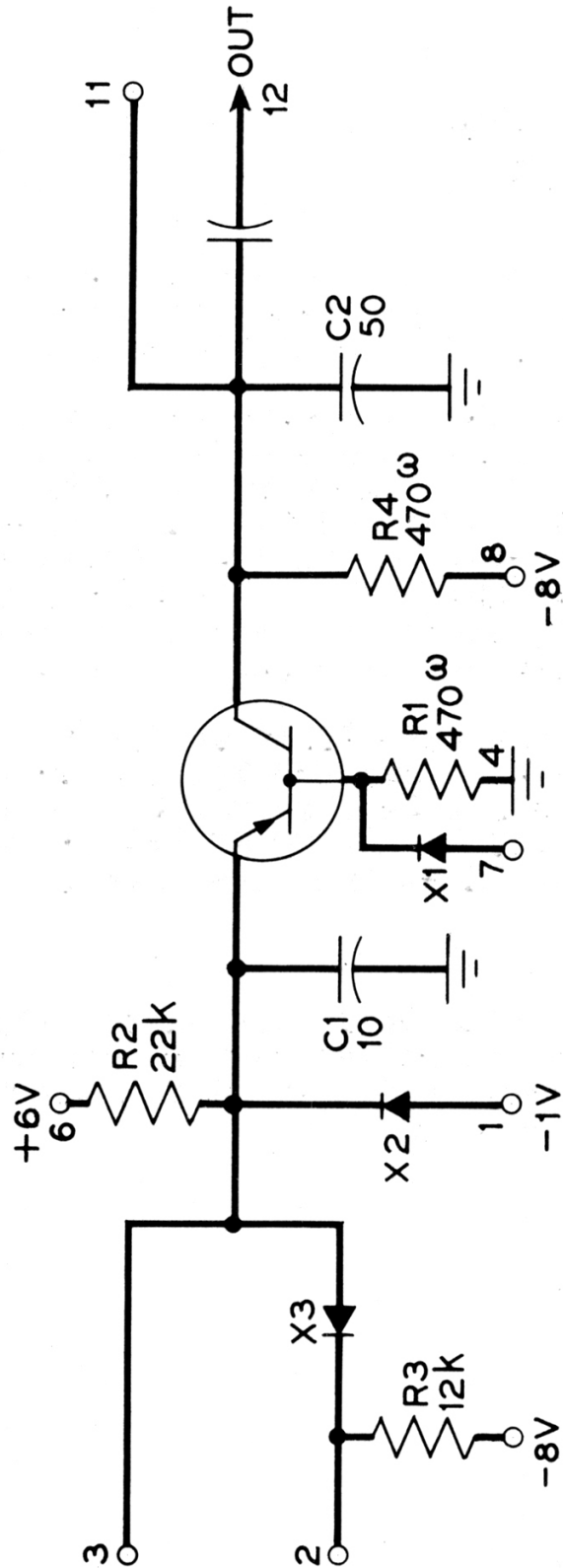


FIG. 9-1

BINARY ADDER

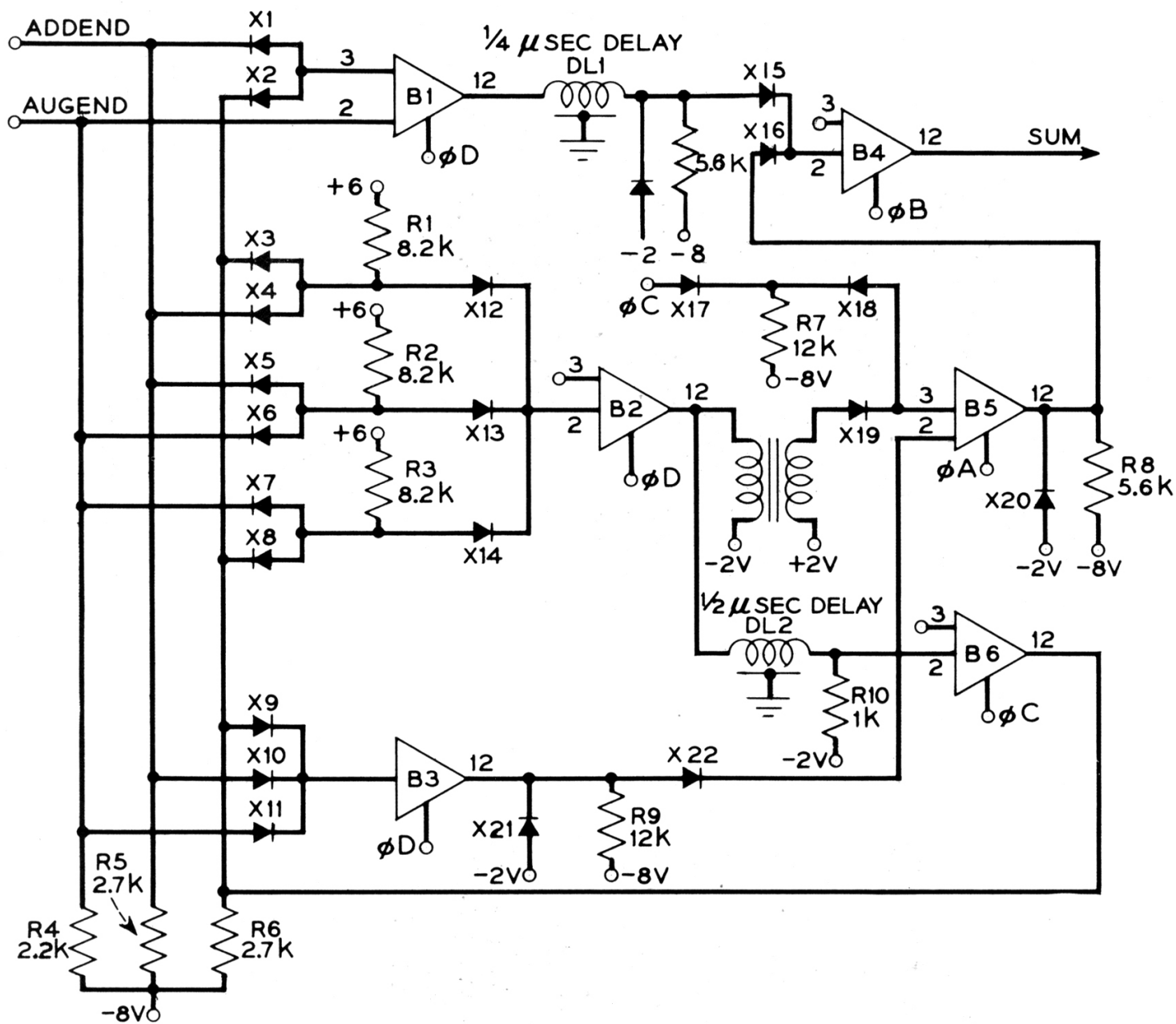
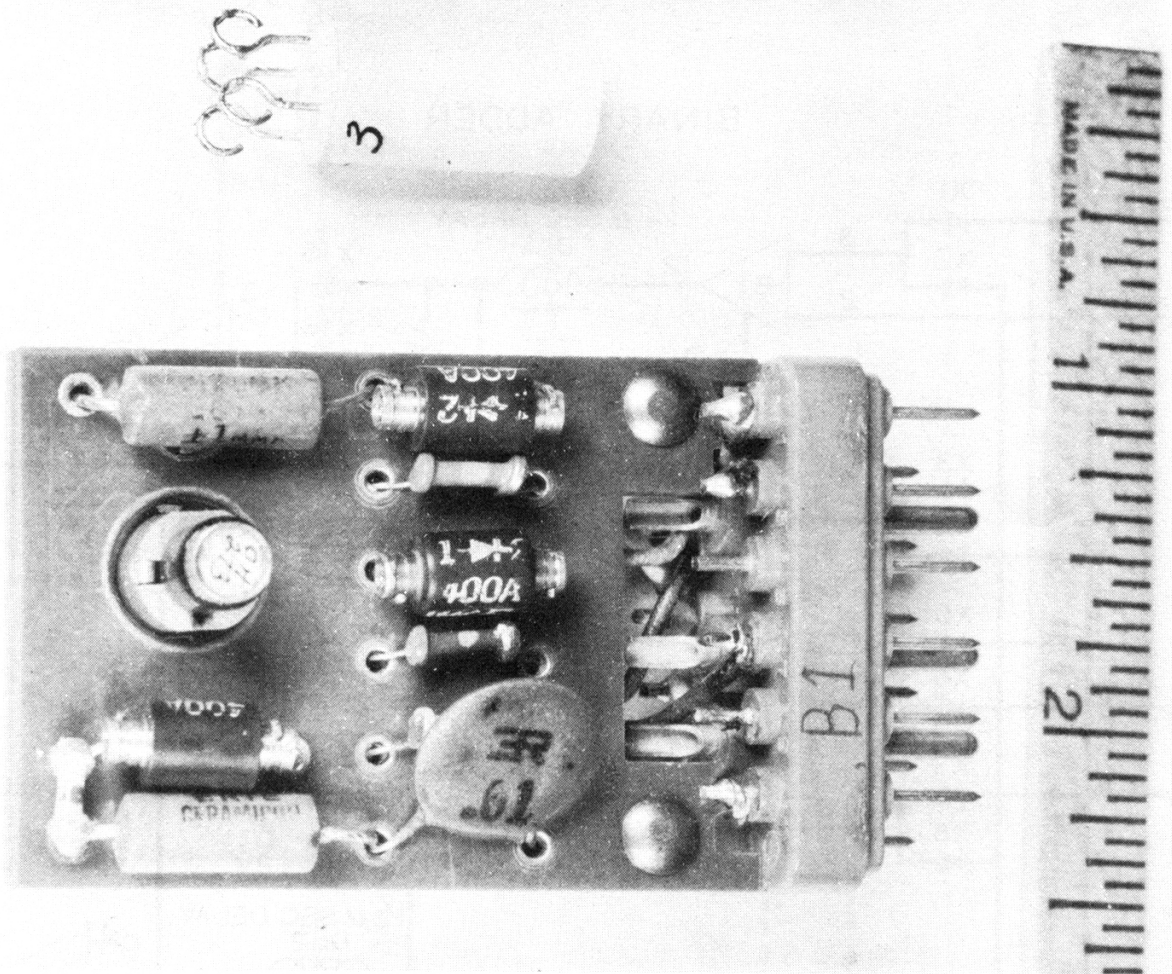


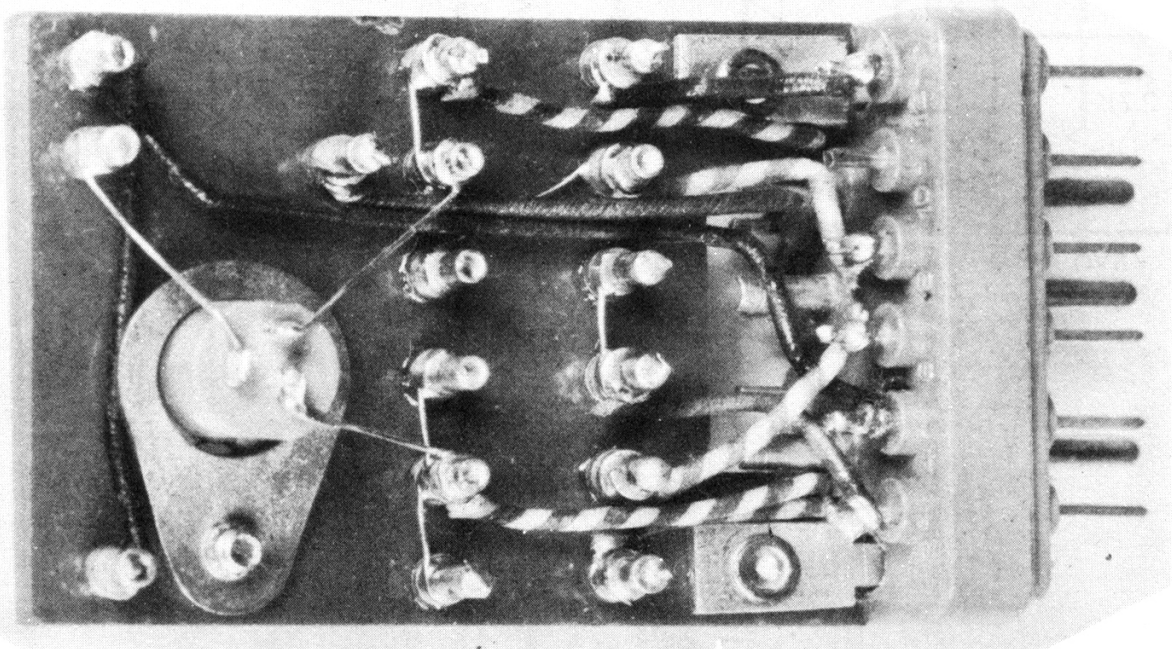
FIG. 9-2

BASIC AMPLIFIER FOR BINARY ADDER

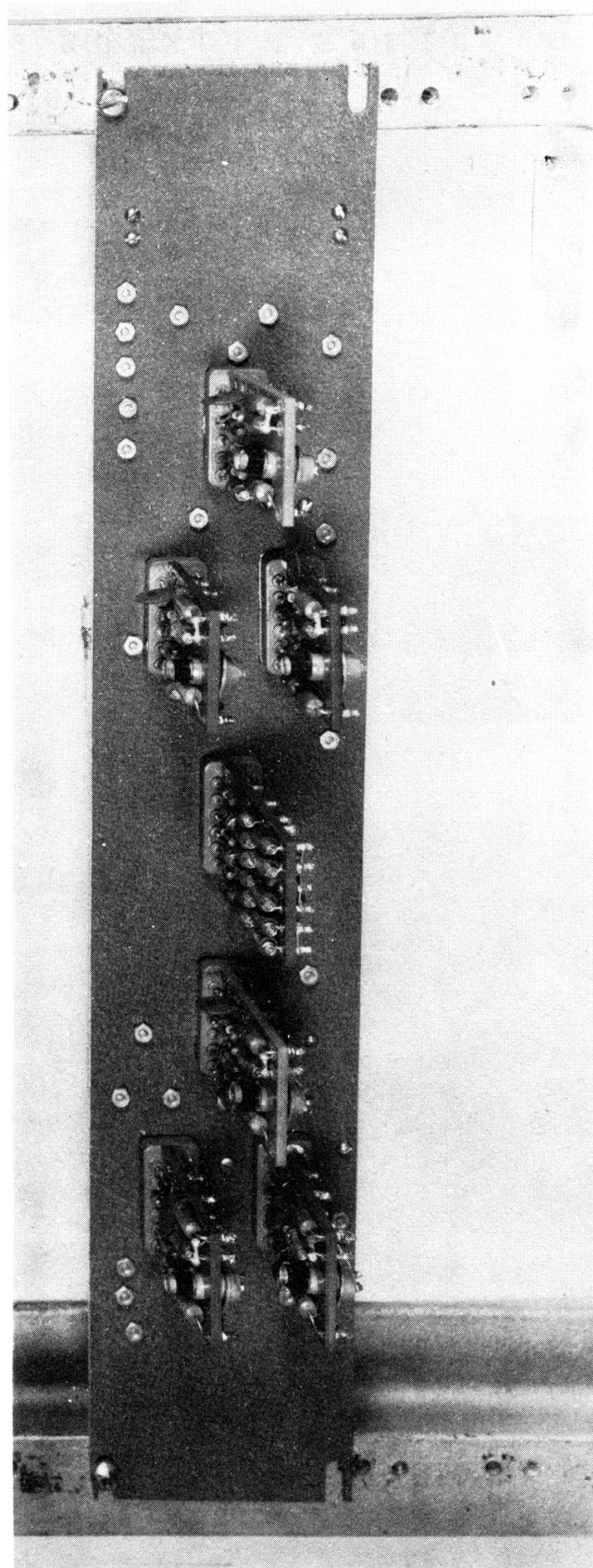
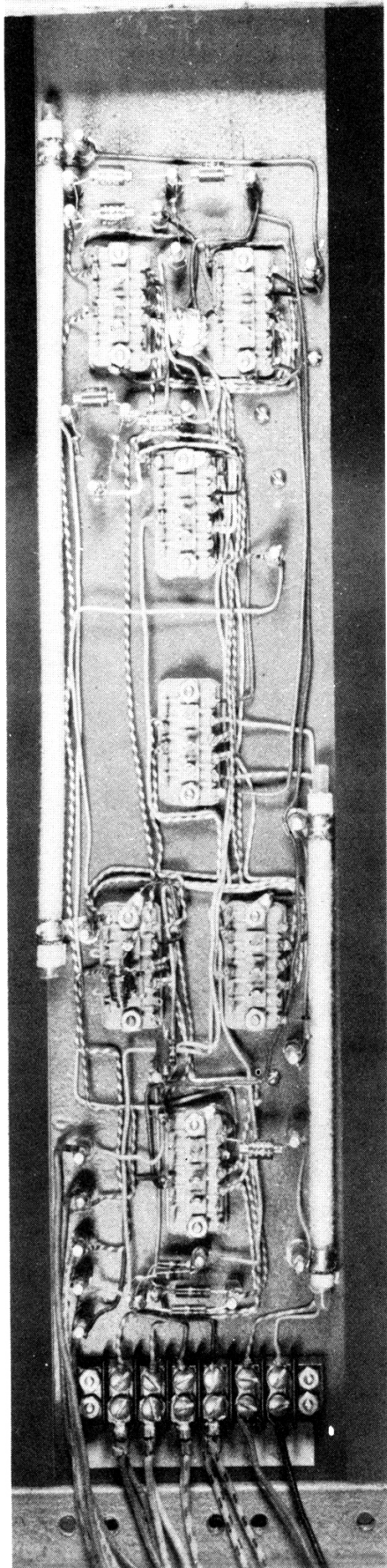
FRONT VIEW



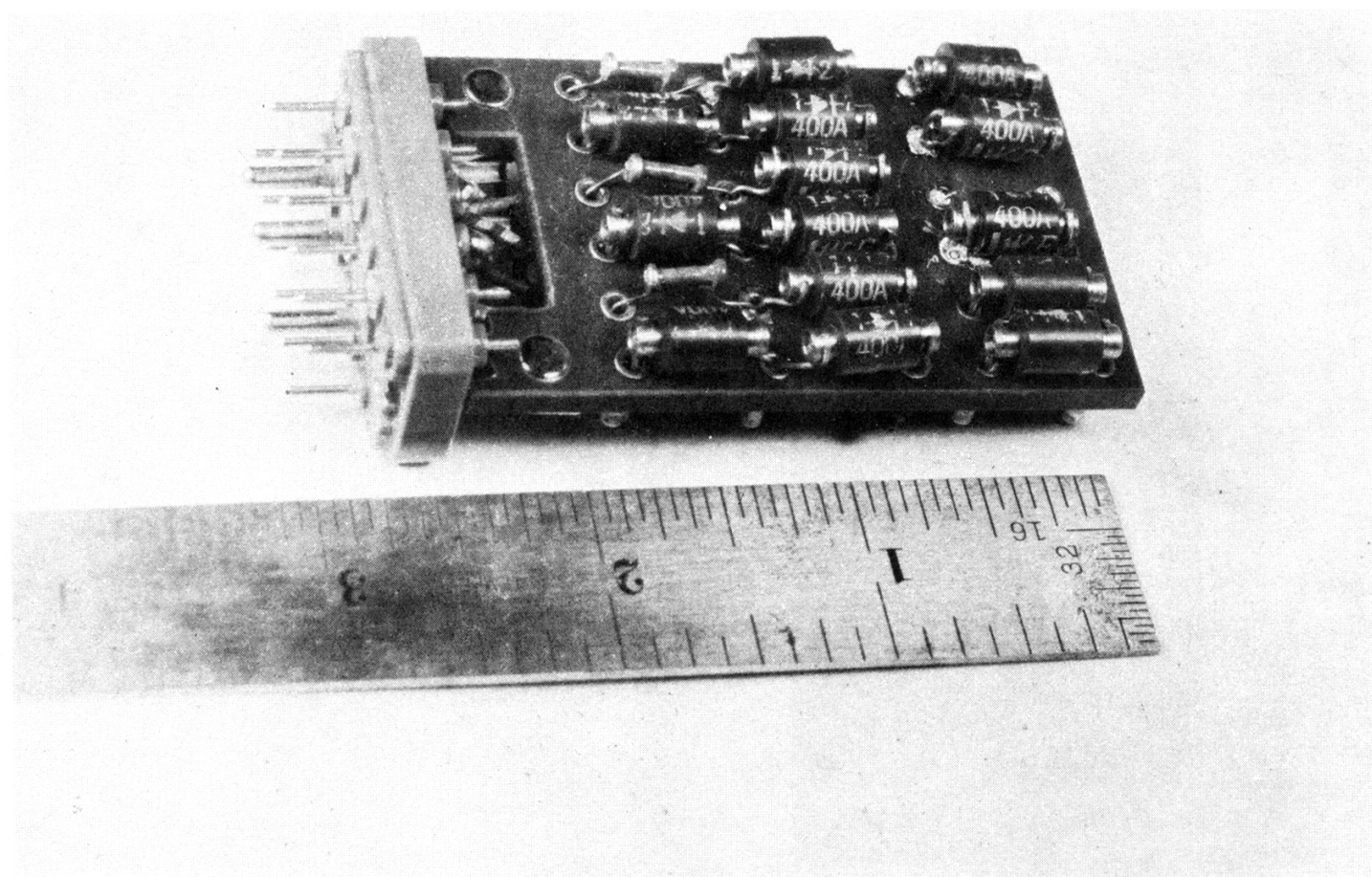
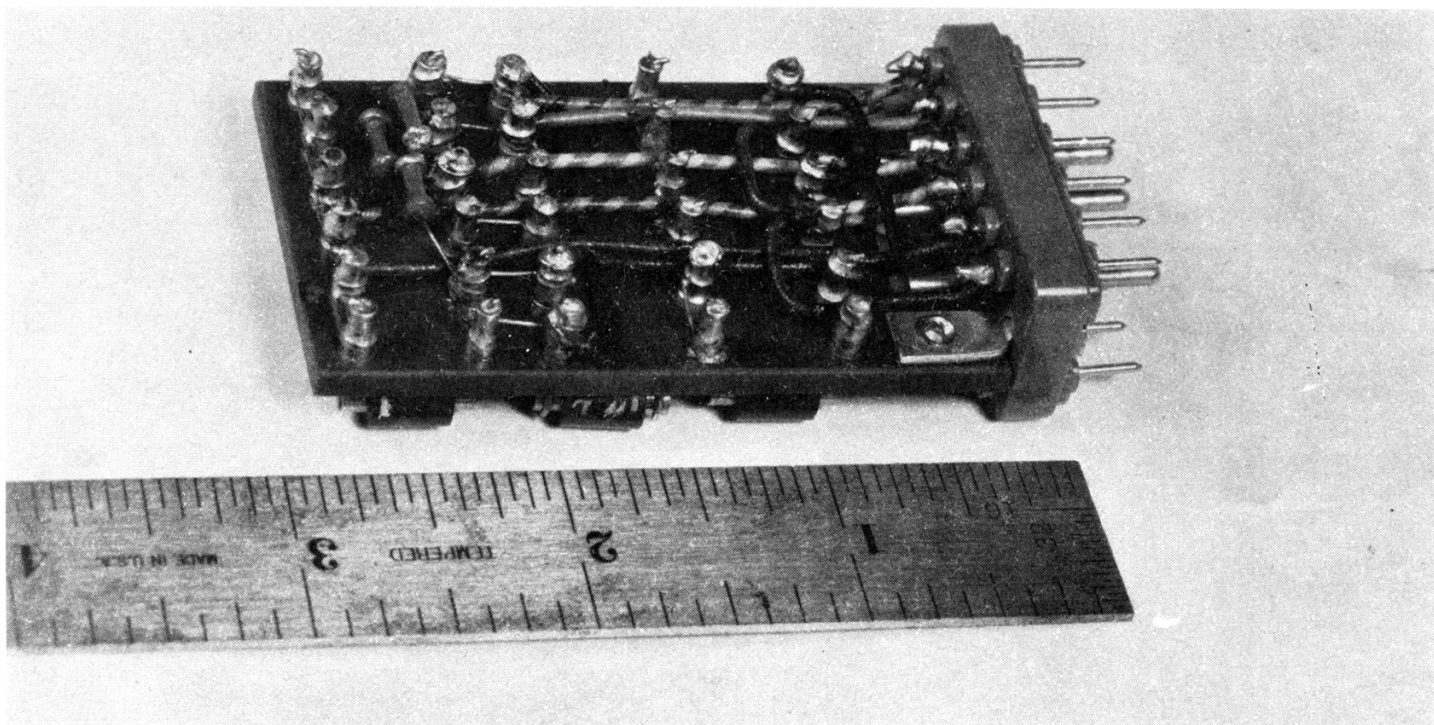
BACK VIEW



B I N A R Y A D D E R
F R O N T A N D R E A R V I E W S



DIODE PACKAGE FOR BINARY ADDER
FRONT AND BACK VIEWS



ADDER WAVEFORMS

ADDEND

AUGEND

CARRY

SUM (DELAYED)

= 10010110110001

= 01011110010011

= 110001111010101
2⁰2¹2²2³2⁴2⁵ ETC

COLLECTOR 3

COLLECTOR 2

" 1

" 5

FIG.9-3

D A T A O N E X P E R I M E N T A L
T R A N S I S T O R T Y P E S

BTL MI679	POINT-CONTACT TRANSISTOR	J. J. KLEIMACK
W.E.CO. A1698	POINT-CONTACT TRANSISTOR	
BTL MI725 - BTL MI729	POINT-CONTACT TRANSISTOR	R. J. KIRCHER R. M. RYDER
BTL MI727 - BTL MI728	P-N JUNCTION DIODES	JOHN N. SHIVE
BTL MI734	POINT-CONTACT TRANSISTOR	B. G. FARLEY
BTL MI740	P-N JUNCTION PHOTOCELL	JOHN N. SHIVE
BTL MI752	NPN JUNCTION TRANSISTOR	K. D. SMITH
BTL MI754 - BTL MI755	P-N JUNCTION DIODES	JOHN N. SHIVE

DATA ON EXPERIMENTAL TRANSISTOR TYPES

It is now possible on an exploratory development level, to make transistors to several sets of prescribed characteristics with good tolerances and satisfactory yields:

For applications involving one or more of the following features, transistors may be especially suitable.

- 1) Economy of Space - Minaturization
- 2) Economy of Power
- 3) Ability to Stand Shock and Vibration
- 4) Long Life

Current transistors have certain limitations as to frequency, power and temperature range. However, with better understanding and improved techniques, it is expected that these will be, at least partially, overcome. Some indication of what may be expected from transistors may be had from inspection of the tables below:

REPRODUCIBILITY

Point Contact Transistors

α	$\pm 20\%$
r_c	$\pm 30\%$
r_e	$\pm 20\%$
r_b	$\pm 25\%$
Cut-off frequency	$\pm 30\%$
Noise figure	$\pm 3\text{db}$
Large signal characteristics	$\pm 25\%$

PERFORMANCE

LOW-FREQUENCY GAIN	<45 db/stage	1752
VIDEO GAIN	20 db/stage	1729
I-F GAIN	20 db/stage	1734
GAIN CONTROL		1752
POWER - CLASS A	20-50 mw	1729, 1752
CLASS B	400 mw	1729
CLASS C	1-3 watts peak	1689, 1698
FREQUENCY RESPONSE	1-3 mc	1752
	7 mc	1729
	20 mc	1734
NOISE FIGURE, 1 kc	15 db	1752
	45 db	1768
LIFE	>70,000 hours	PT. CONTACT UNITS
TEMPERATURE RANGE	<80°C	1729
VIBRATION	>100 g	PT. CONTACT UNITS
SHOCK	~20,000 g	PT. CONTACT UNITS
UNIFORMITY	±30%	PT. CONTACT UNITS
SIZE	$\frac{1}{1000}$ cu. in.	1689
	$\frac{1}{100}$ cu. in.	1752
	$\frac{1}{50}$ cu. in.	CASED UNITS
MINIMUM POWER	1 microwatt	1752
	few milliwatts	1768
NEGATIVE RESISTANCE		1689, 1698, 1734
NEGATIVE FEEDBACK		1752

A more detailed discussion is given below.

Gain: At audio and carrier frequencies, gain up to about 45 db per stage is offered by the 1725 junction-type unit in grounded emitter connection. At video frequencies, gain of about 20 db per stage is offered by the 1729 point contact unit in grounded base connection. Even though the grounded emitter connection can give somewhat more gain, it is the

moment not recommended for point-contact transistors because of stability and variability difficulties. At high frequencies (up to about 20 mc/s) the 1734 point contact unit offers some possibility of gain of about 20 db per stage; but stability problems make this use more exploratory than the 1729 or 1752.

Gain Control: Transconductance proportional to operating current is offered by the 1752 units.

Power Output:

a) Undistorted Class A power output from either 1752 or 1729 is about 20 to 50 mw. The 1752 has higher efficiency, but only slightly more gain.

b) Class B output of about 400 milliwatts has been obtained from a pair of 1729's in push-pull connection, using duality-type circuitry. The collector power efficiency is good, but the overall efficiency may be debilitated if a resistor is used in the power supply circuit. Data on 1752's is not available, but they would probably give about the same output with somewhat better gain and considerably better overall efficiency.

c) Class C output with rectangular wave-forms in on-off trigger-type service permits efficiency well above 90%. Consequently 1698 units can give powers in the range 1 to 3 watts peak.

Relative to what can be obtained from tubes, power output is lower but efficiency is often considerably higher.

Frequency Response: The 1752 can be operated up to about 3 megacycles as a grounded base video amplifier: up to only about 200 kilocycles in the higher-gain grounded-emitter connection. The point contact 1729 units average 7 megacycles cutoff frequency; the point-contact 1734 units average about 20 megacycles, but with more feedback, so that the last are useful primarily in trigger circuits. These frequency figures are quite variable at present, but by selection a range of $\pm 30\%$ can be met by 1729 units.

Noise: A noise figure of about 15 db at 1000 cycles for the 1752, with $1/f$ frequency response, is indicated by very preliminary data. Noise of point contact units is about 30 db higher.

Vibration and Shock: Vibration to at least 100 g does not affect units and shock to the order of 20,000 g does not damage them. In applications where vibration is severe, even point contact transistors may give noise performance superior to tubes.

Size: At present only the 1689 and 1752 units are available in beads. (Less than .01 cubic inch volume). However, in many applications the overall size is limited by passive components, even for cased transistors (1/50 cubic inch), which are about an order of magnitude smaller than comparable tubes.

Power Economy: Operation with only microwatts of input is possible with 1752 junction-type units. The 1768 point-contact units give 20% efficient oscillations at 35 milliwatts input, and will operate with less.

Low Voltage Operation: For 1752's a few tenths of a volt bias and a few microamperes of current will produce operation; for 1768's, a volt or two, with about a hundred microamperes, is needed.

Life: Extrapolated estimates give about 70,000 hours or more for the life of point-contact units under moderate operating conditions. Data are not available for junction units, but comparable diodes indicate even better performance is likely.

Uniformity: Units are held to limits which are in most cases within 20 to 30 per cent of nominal values for the type. These figures are comparable with the ordinary run of unselected vacuum tubes, and are sufficient for a useful degree of interchangeability. For example, the range of gain of 1729 grounded-base amplifiers is about ± 1.5 db from nominal.

Miscellaneous Circuit Properties:

a) Negative feedback for extreme uniformity and low distortion is applicable, especially to 1752 amplifiers.

b) A useful high-to-low impedance transformation, similar to the cathode-follower tube, is offered by the analogous connection of the 1752.

c) Negative resistance effects obtainable from point contact units, especially the 1689 and 1698, are very useful in trigger-type switching circuitry.

d) Stability of the operating point, particularly in transistors having alpha greater than one, requires attention to terminating impedances at all frequencies, including those outside the useful band, both high and low. In particular, self-biasing requires care because the bias polarity corresponds to positive rather than negative d-c feedback. To reduce variations in operating point, it is well to have the d-c resistance in the emitter lead much larger than that in the base lead.

Finally, there follows information on a number of transistor types which are either in pilot production or in an advance development stage.

M1689 TRANSISTOR

DEVELOPMENT CHARACTERISTICS OF TRANSISTOR TYPE B.T.L. M1689

The M1689 bead transistor is a miniaturized transistor having electrical characteristics suitable for switching circuits. It consists of a molded bead, approximately one-eighth inch in diameter, with a heavy base lead and two fine wires as the emitter and collector connections. It is primarily for use in miniaturized molded circuits in which small size and direct connection into circuits by soldering is required. Application may also be made without potting.

An exploratory development specification for the transistor is attached.

EXPLORATORY DEVELOPMENT SPECIFICATIONS

Description: Transistor - Switching Applications

<u>Ratings:</u>	V_c	I_c	V_e	I_e	P_c	T_a	Note 1
Absolute	V	mA	V	mA	mW	°C	
Maximum	-50	-40	-40	+40	80		

Test Conditions: - - - - - 25

Dimensions: Dia. 1/8" Approx. Mounting Position: Any

Connections: Base - .025" Dia. Wire

Collector - Bent Lead - .005" Dia.

Emitter - Straight Lead - .005" Dia.

<u>Test</u>	<u>Conditions</u>	<u>Min.</u>	<u>Max.</u>
Handling Precautions	Note 2		
Aging Period	48 hrs., Note 6		
Vibration & Shock	Note 3		
OFF Collector Current	$V_c = -35V$ dc; $I_e = 0$ Note 7	$I_c:0$	-2 mA dc
ON Collector Voltage (1)	$I_c = -2$ mA dc; $I_e = 1$ mA dc; Note 4	$V_c:0$	-3 V dc
ON Collector Voltage (2)	$I_e = 3$ mA dc; $I_c = -5.5$ mA dc	$V_c:0$	-4 V dc
Emitter Resistance	$V_e = -10V$ dc	$I_e:0$	-0.2 mA dc
Alpha (1)	$V_c = -30V$ dc $I_e = +1.0$ mA dc Note 5	$\alpha:1.5$	
Alpha (2)	$V_c = -30V$ dc; $I_e = +0.5$ mA dc Note 5	$\alpha:2.0$	-
Alpha (3)	$V_c = -30V$ dc; $I_e = -0.1$ mA dc Note 5	$\alpha: -$	0.3
Open Circuit Input Resistance	$V_c = -10V$ dc; $I_e = +1$ mA dc	$r_{11}: -$	800 Ohms
Open Circuit Feedback Resistance	$V_c = -10V$ dc; $I_e = +1$ mA dc	$r_{12}: -$	500 Ohms
Open Circuit Forward Resistance	$V_c = -10V$ dc; $I_e = +1$ mA dc	$r_{12}:15,000$	- Ohms
Open Circuit Output Resistance	$V_c = -10V$ dc; $I_e = +1$ mA dc	$r_{22}:10,000$	- Ohms
Turn-Off Time	Note 8	0	1 microsecond

- Note 1 In ward direction of current is taken as positive for both emitter and collector. Voltages are measured with respect to the base. Subscripts "c" and "e" refer to collector and emitter respectively. Voltages are taken on an absolute basis so that a voltage of $V_c = -40$ is greater than a voltage of $V_c = -30$ volts. DC ratings are on the basis of any duration longer than the order of 5 microseconds. Transients in excess of the ratings, but with durations much less than 5 microseconds, may not injure the unit; it is to be understood, however, that such service is experimental. Currents of 50-100 mA have been employed.
- Note 2 The transistor should not be subjected to service in which there may be excessive transients as in plugging in and out with power on, but this may be done if under any case the ratings are not exceeded. Base contact should be made first. If solder connections are made, heat sink protection on the transistor side of the joint should be provided as with flat nose pliers.
- Note 3 The same degree of ruggedness experienced with germanium diodes may be expected. Transistors have been shocked and accelerated to 20,000 G without failure.
- Note 4 Limiting resistors of 100,000 ohms in the emitter circuit and 50,000 ohms in the collector circuit should be employed.
- Note 5 Alpha tests (1), (2) and (3) are small signal measurements.
- Note 6 All tests should be made after aging at 75mW, collector dissipation for 48 hours and after four temperature cycles of one-half hour duration between room temperature and 75°C.
- Note 7 For the I_{co} test, -35 V from a constant voltage source should be applied for at least 5 minutes at the end of which period I_{co} is not to exceed -2 mA. I_c shall be not greater than -2 mA at $V_c = -20$ volts at 55°C.
- Note 8 This test and requirement is measured in the circuit shown in Fig. 13-1 and is defined as the time required for the collector voltage to return to the value it had in the ON condition also illustrated. The transistor is in a "fully saturated" ON state when the turn-off step is applied. The emitter and collector currents are equal in the ON state. (This is a tentative method for measuring turn-off time.)

J. J. KLEIMACK

TEST FOR TURN-OFF TIME

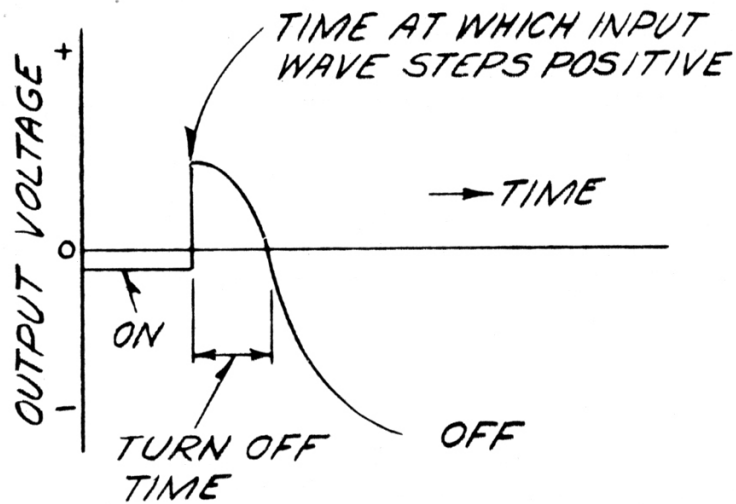
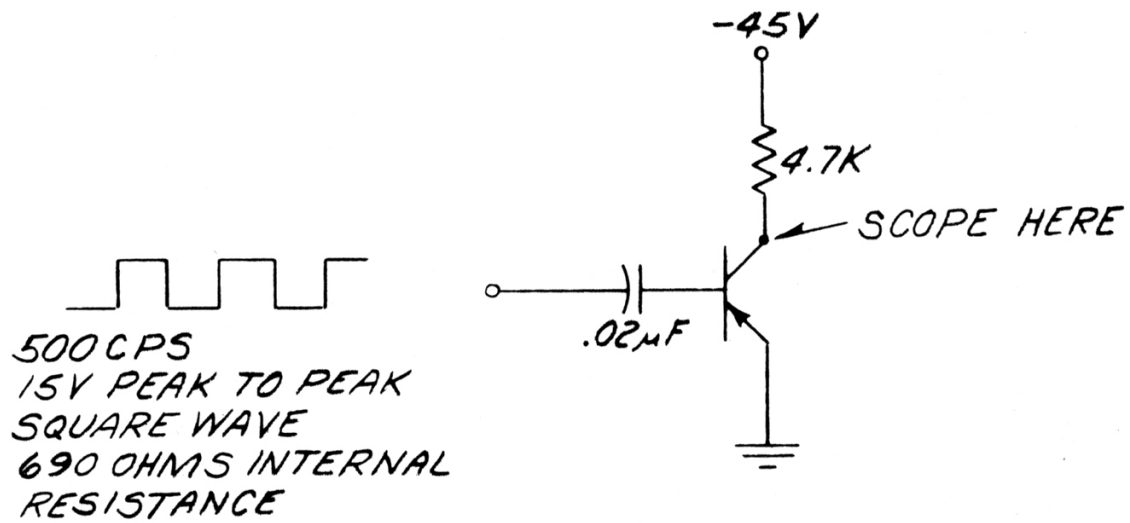
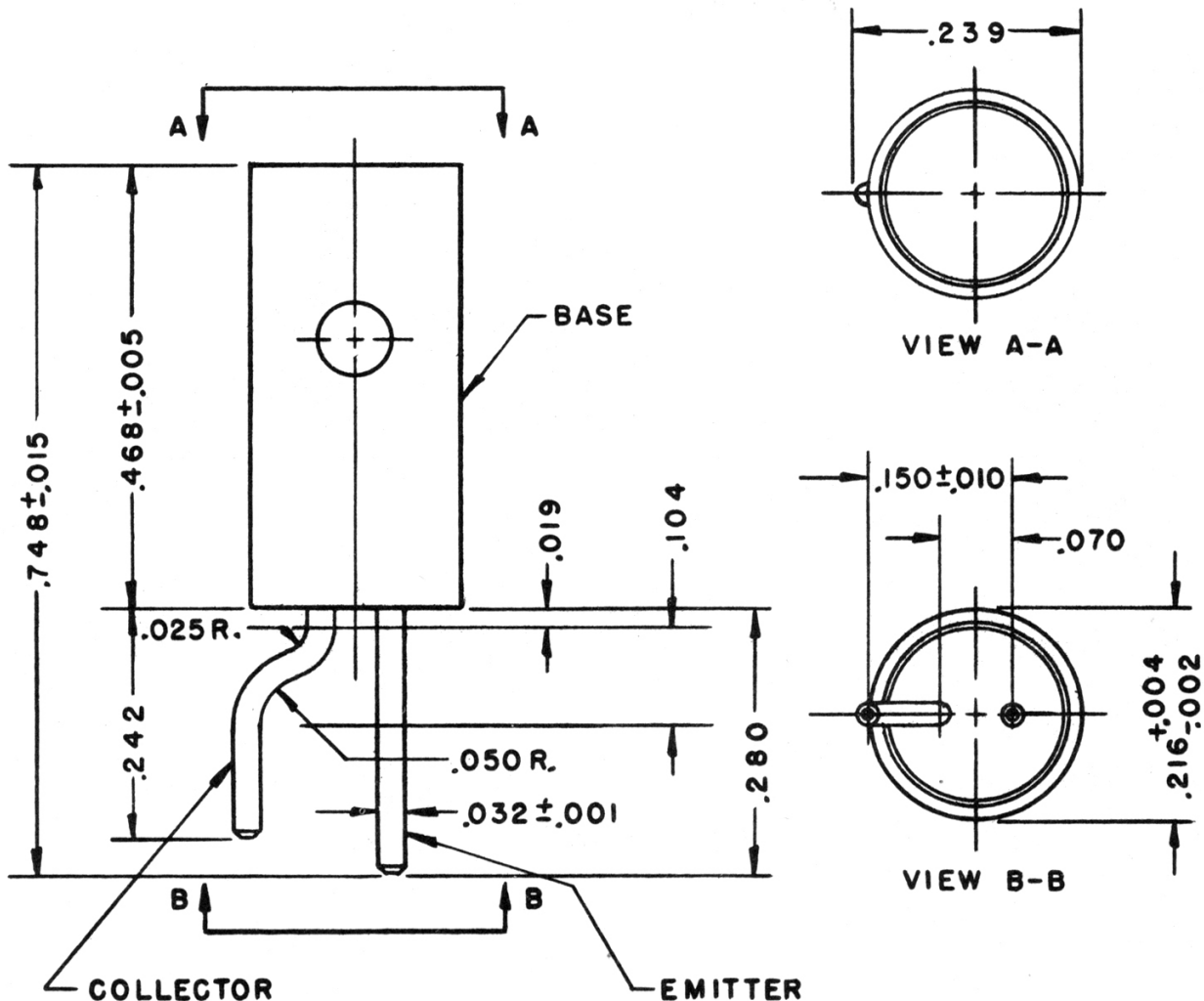


FIG.13-1

ADVANCE TRANSISTOR DATA SHEET
WESTERN ELECTRIC TRANSISTOR
DEVELOPMENT MODEL A1698



DESCRIPTION

The A1698 is a point contact transistor triode in cartridge form. It is designed for use in switching circuits where the large-signal parameters of the active device are of primary interest. The external connections are arranged to fit the Cinch #EXP8672 or equivalent socket.

(Operating conditions and characteristics on Pages 2 and 3)

Issue 1, 9-7-51

A1698

GENERAL CHARACTERISTICS

MECHANICAL DATA

Mounting Position - - - - - any
Dimensions and Pin Connections - See Outline, Page 1

MAXIMUM RATINGS

Collector Voltage (D-C)	- - - - -	-100 volts
Collector Current (D-C)	- - - - -	-15 milliamperes
Collector Dissipation	- - - - -	120 milliwatts
Emitter Voltage (D-C)	- - - - -	-100 volts
Emitter Current (D-C)	- - - - -	15 milliamperes
Ambient Temperature	- - - - -	130 F

TYPICAL OPERATING CONDITIONS AND CHARACTERISTICS

Stable End Points

High Collector Impedance Condition

Emitter Current (D-C)	- - - - -	0 milliampere
Collector Voltage (D-C)	- - - - -	-40 volts
Collector Current (D-C)	- - - - -	-1.5 milliamperes

Low Collector Impedance Condition

Emitter Current (D-C)	- - - - -	1 milliampere
Collector Current (D-C)	- - - - -	-2 milliamperes
Collector Voltage (D-C)	- - - - -	-2 volts

Small Signal Characteristics

Current Amplification

When Collector Voltage=-30; Emitter Current=1ma	- - -	2
When Collector Voltage=-30; Emitter Current=0.05ma	- -	3
When Collector Voltage=-40; Emitter Current=-0.1ma	- -	0.2
Cut-off Frequency, Nominal ¹	- - - - -	5 megacycles

Base Resistance, Nominal² (r_{12})

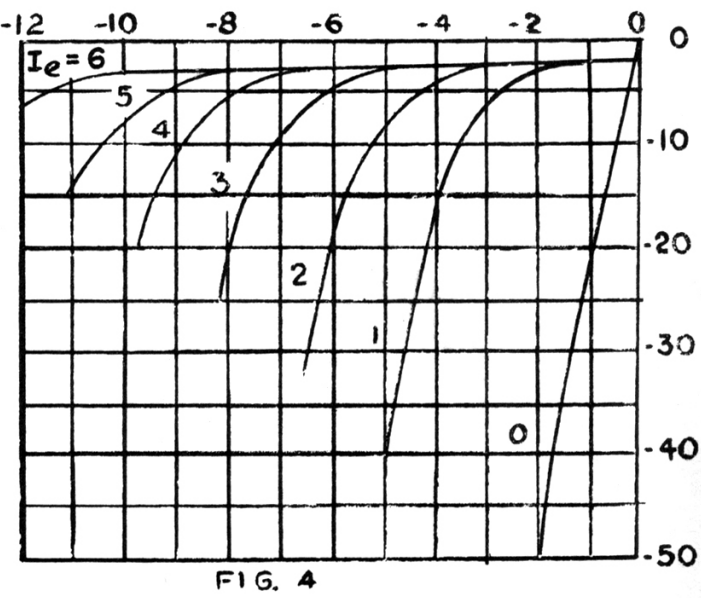
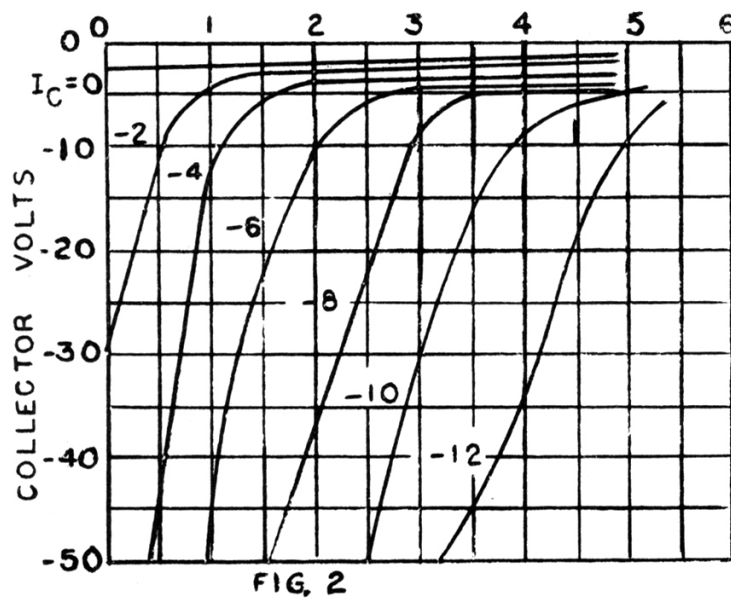
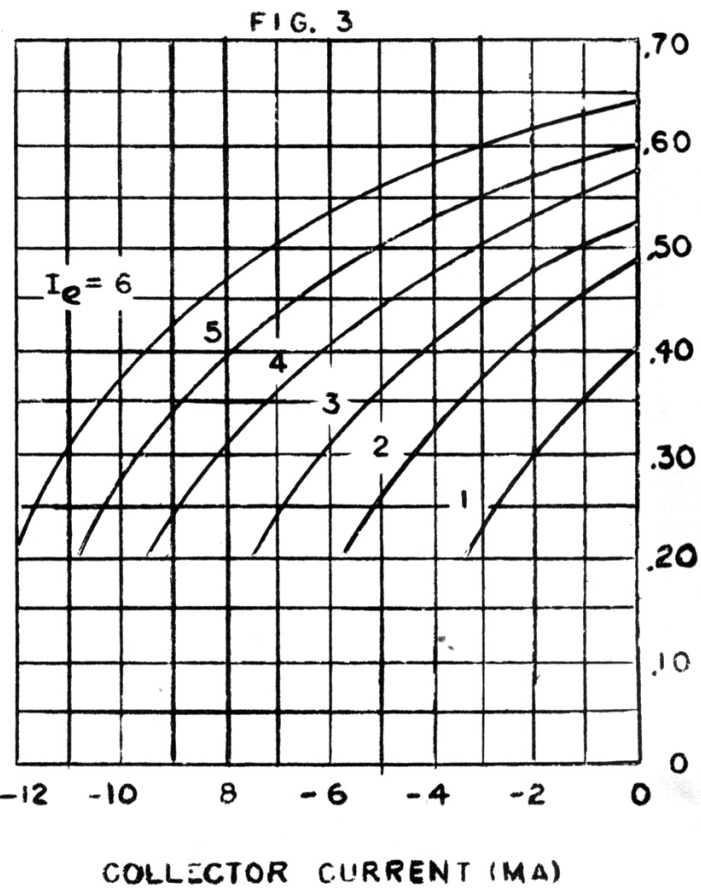
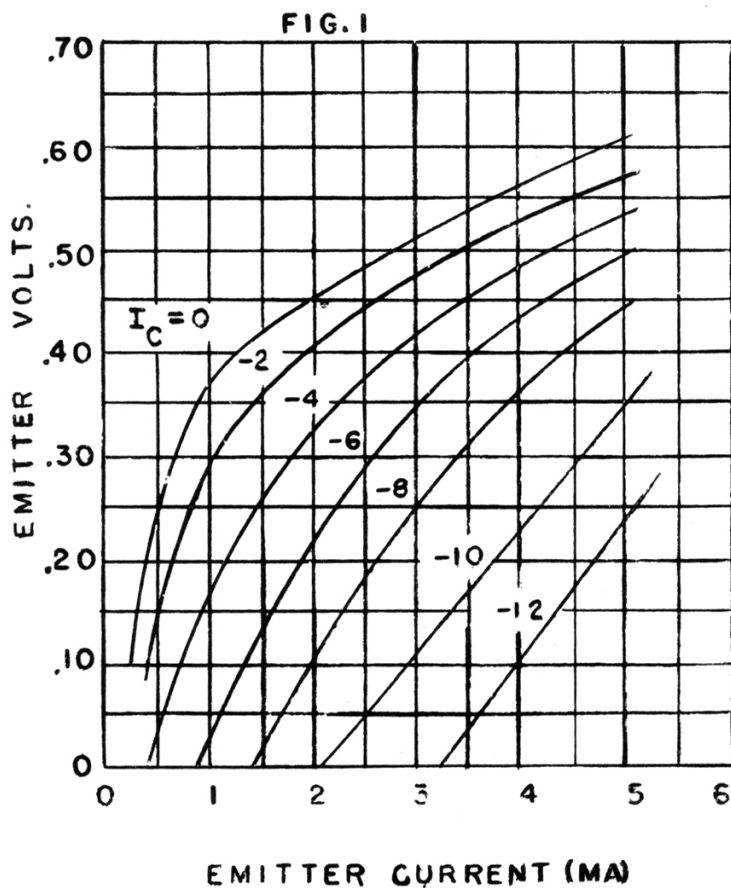
At $V_c = -30$; $I_e = 1.0$ ma	- - - - -	200 ohms
---------------------------------	-----------	----------

Note 1 Cut-off is defined as the frequency at which the current amplification is 3 db below its low frequency value.

Note 2 Base resistance is defined as the ratio of the voltage developed across the input terminals, to the collector current causing it. In other words, it is a measure of the positive feed back inherent in this type of device.

Operating Precaution

Where possible the transistor should not be connected to its circuit with bias voltages applied. Where this is not possible, the base connection should always be made first. Violation of this precaution may result in permanent damage to the transistor.



EXPLORATORY DEVELOPMENT CHARACTERISTICS OF

BTL M1725, BTL M1729 TRANSISTORS

Recent improvements in uniformity of transistors have permitted exploratory production of units with variations within about $\pm 25\%$ of nominal characteristics. While this degree of uniformity is somewhat inferior to that of standardized vacuum tubes, a useful degree of interchangeability is now realizable. Temporary specifications on two types of transistors, the BTL M1729 and the BTL M1725 are attached herewith.

For general purpose audio and carrier frequency application, the BTL M1729 unit has 20db gain, 50mw class A output power, 3 mc. high frequency cutoff, and 54db noise figure (at 1000 cycles).

For economical low voltage operation, the BTL M1725 unit has 18db gain, 20% output power efficiency, 48db noise figure (1000 cycles), with only 4ma at 5 volts required of the power supply.

At ambient temperatures approaching 60°C the properties of these transistors may be adversely affected, the units are therefore given reduced dissipation ratings above 50°C ambient, and are not recommended for operation above 80°C ambient temperature.

The predicted life of these units, when operated at 125 milliwatts dissipation, (before the gain falls 3db) is of the order of 70,000 hours.

The same degree of ruggedness experienced with germanium diodes may be expected. Accelerations up to 10,000 G in any direction can be tolerated by these transistors.

EXPLORATORY DEVELOPMENT SPECIFICATIONS

BTL M-1725 TRANSISTOR

Reference - JAN-1A

Description - Transistor

Maximum Ratings (Note 1)

V_c	I_c	V_e	I_e	P_c	P_e	Ambient
V	ma	v	ma	mW	mW	$^{\circ}\text{C}$
-50	-20	+5	+15	200	50	50 (Note 4)

Test Conditions

-5.0

+1.5

20

Dimensions: Per Outline 2

Mounting Position: Any

Connections: Per Outline 2

<u>Test</u>	<u>Conditions</u>	<u>Min.</u>	<u>Max.</u>
Handling Precautions	Note 2		
Holding Period (48 Hours)	Note 5		
Vibration and Shock	Note 3		
Input Resistance R_{11}	Note 6	160	230 ohms
Feedback Resistance, R_{12}	Note 6	90	160 ohms
Forward Resistance, R_{21}	Note 6	12000	24000 ohms
Output Resistance R_{22}	Note 6	6000	12000 ohms
Current Amplification Factor, α	Note 6	1.8	2.6
Noise figure (1000 cycles)	Note 7	----	53 db
Frequency cutoff (alpha 3db down)		3.0	---- mc

Note 1 Subscripts c and e refer to collector and emitter respectively. Voltages are measured with respect to the base. DC ratings are on the basis of any duration longer than about 5 microseconds. Transients of shorter duration somewhat in excess of the ratings may not injure the unit; it is to be understood, however, that such service is experimental.

Note 2 The transistor should not be subjected to excessive transients such as may occur on plugging in or out with power on. This may be done if in any case the ratings are not exceeded; base contact should be made first. If solder connections are made, heat sink protection on the transistor side of the joint should be provided, as with flat-nose pliers. It is recommended that solder connections not be made to the base.

- Note 3 The same degree of ruggedness experienced with germanium diodes may be expected. Transistors have been shocked and accelerated to 20,000 G with no difficulties, except that an acceleration of more than 10,000 G, applied in such a direction as to lift the points, may cause failure. Suitable packaging is used to protect the units against normal atmospheric conditions.
- Note 4 For ambient temperatures from 50°C to 80°C, the maximum collector dissipation should be 100 milliwatts.
- Note 5 All tests should be made after holding period.
Ref. F3, JAN-1A.
- Note 6 Operating point for measurement of circuit parameters is $I_e = 1.5 \text{ ma}$, $V_c = -5\text{v}$.
- Note 7 Noise figure varies inversely with frequency.

EXPLORATORY DEVELOPMENT DATA SHEET

BTL M-1725 TRANSISTOR

Triode Amplifier for Minimum Power Drain

MAXIMUM RATINGS not to be exceeded in continuous operation

Emitter Current, I_e	15 ma
Emitter Voltage, V_e	-50 v
Emitter Dissipation	50 mW
Collector Current, I_c	-20 ma
Collector Voltage, V_c	-50 v
Collector Dissipation	200 mW (up to 50°C ambient)
	100 mW (up to 80°C ambient)

AVERAGE OPEN CIRCUIT RESISTANCE PARAMETERS

Grounded base connection, with	$I_e = 1.5 \text{ ma}$, $V_c = 5.0 \text{ v}$
Input Resistance	$R_{11} = 195 \text{ ohms}$
Feedback Transfer Resistance	$R_{12} = 115 \text{ ohms}$
Forward Transfer Resistance	$R_{21} = 16,000 \text{ ohms}$
Output Resistance	$R_{22} = 8,000 \text{ ohms}$
Current Amplification Factor	$a = 2.1$

TYPICAL LOW-DRAIN OPERATION CONDITIONS

Class A power amplifier, grounded base conditions

Emitter Current, I_e	1.5 ma
Emitter Dissipation	less than 1 mW
Collector Voltage, V_c	-5 v
Collector Current, I_c	-4 ma
Collector Dissipation	20 mW
Input Termination	500 ohms
Output Termination	1000 ohms
Available Power Gain	18 db
Power Output	4.5 mW
Cutoff Frequency (alpha 3db down)	5 mc
Noise Figure (1000 cycles)	48 db

Dimensions:

Outline drawing Fig. 14-1

EXPLORATORY DEVELOPMENT SPECIFICATIONS

BTL M-1729 TRANSISTOR

Reference - JAN-1A

Description - Transistor

Ratings:	V_c	I_c	V_e	I_e	Load	Dissipation		Ambient
	Units	Volts	ma.	Volts	ma.	Ohms	Milliwatts	Temperature degrees, C
Maximum	-50	-20	+5	+15		50	200	50 (Note 4)
Test Conditions (small signal)	-30		+1.0		20,000			Approx. 30

Dimensions: Per Outline 2 Mounting Position: Any

Connections: Per Outline 2

<u>Ref.</u>	<u>Test</u>	<u>Conditions</u>	<u>Min.</u>	
	Handling	Note 3		
	Precautions	Note 2		
F3	Holding Period	48 hrs., Note 5		
	Vibration and Shock	Note 3		
	Collector Voltage	-30V, Emitter Current 1.0 ma.		
	Input Resistance,	R_{11}	150 ohms	225 ohms
	Feedback Transfer Resistance,	R_{12}	30	100
	Forward Transfer Resistance,	R_{21}	20,000	40,000
	Output Resistance,	R_{22}	10,000	20,000
	Current Amplification Factor,	α	2.0	3.0
	Cutoff Frequency, f_c		4.0	--mc
	Noise Figure (1000 cycles)	(Note 7)	--	56.0 db

Note 1 Subscripts c and e refer to collector and emitter respectively. Voltages are measured with respect to the base. DC ratings are on the basis of any duration longer than about 5 microseconds. Transients of shorter duration somewhat in excess of the ratings may not injure the unit; it is to be understood, however, that such service is experimental.

Note 2 The transistor should not be subjected to excessive transients such as may occur on plugging in or out with power on. Such plugging in or out may be done if in any case the ratings are not exceeded; base contact should be made first. If solder connections are made, heat sink protection on the transistor side of the joint should be provided, as with flat-nose pliers. It is recommended that solder connections not be made to the base.

- Note 3 The same degree of ruggedness experienced with germanium diodes may be expected. Transistors have been shocked and accelerated to 20000 G with no difficulties, except that an acceleration of more than 10000 G, applied in such a direction as to lift the points, may cause failure. Suitable packaging is used to protect the units against normal atmospheric conditions.
- Note 4 For ambient temperatures from 50°C up to 80°C, the maximum collector dissipation should be 100 milliwatts.
- Note 5 All tests should be made after holding period.
Ref. F3, JAN-1A.
- Note 6 Operating point for measurement of circuit parameters is $I_e = 1.0$ ma, $V_c = -30$ v.
- Note 7 Noise Figure varies inversely with frequency and is measured at $I_e = 0.5$ ma, $V_c = -8$ v.

EXPLORATORY DEVELOPMENT DATA SHEET

BTL M-1729 TRANSISTOR

Triode Amplifier for Audio and Carrier Frequencies

MAXIMUM RATINGS not to be exceeded in continuous operation

Emitter Current I_e	15 milliamperes
Emitter Voltage, V_e	-50 volts to +5 volts
Emitter Dissipation	50 milliwatts
Collector Current, I_c	-20 milliamperes
Collector Voltage, V_c	-50 volts
Collector Dissipation	200 milliwatts (up to 50° ambient)
Collector Dissipation	100 milliwatts (for ambient up to 80°C)

AVERAGE OPEN CIRCUIT RESISTANCE PARAMETERS. GROUNDED BASE CONNECTION AT THE OPERATING POINT $I_c = 1.0$ ma, $V_c = -30$ volts

Input Resistance	$R_{11} = 190$ ohms
Feedback Transfer Resistance	$R_{12} = 75$ ohms
Forward Transfer Resistance	$R_{21} = 32,000$ ohms
Output Resistance	$R_{22} = 15,000$ ohms
Current Amplification Factor	$\alpha = 2.5$

TYPICAL OPERATING CONDITIONS: Small Signal Class A Amplifier

Emitter Current, I_e	1.0 milliamperes
Emitter Dissipation	Less than 1 milliwatt
Collector Voltage, V_c	-30 volts
Collector Current, I_c	5.0 milliamperes
Collector Dissipation	150 milliwatts
Input Termination	300 ohms
Available Power Gain	20 db
Load Resistance	15,000 ohms
Cutoff Frequency (alpha 3 db down)	5 Mc
Noise Figure (1000 cycles)	54 db

Dimensions:

Outline drawing Fig. 14-1

NOTE Noise Figure is inversely proportional to frequency. In operation at $I_e = 0.5$ ma, $V_c = 8$ volts, the noise figure improves to 48 db.

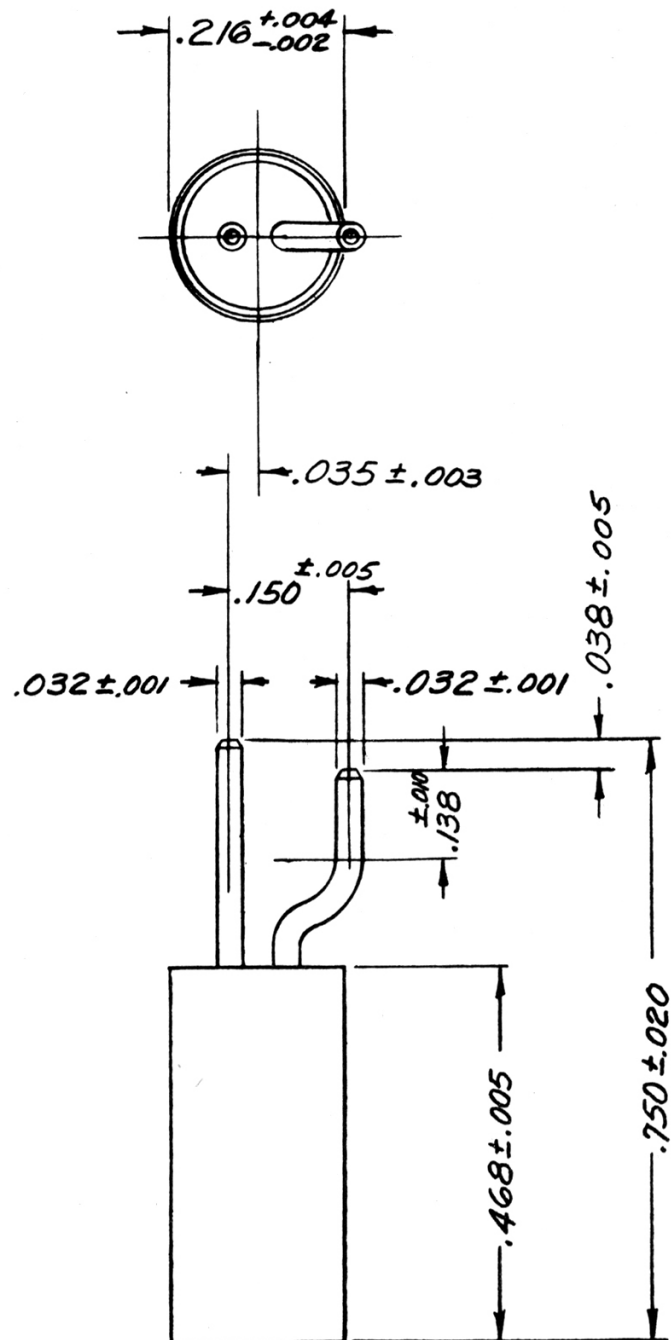
TYPICAL OPERATING CONDITIONS: Large Signal Class A Amplifier

Emitter Current, I_e	2.0 milliamperes
Emitter Dissipation	Less than 2 milliwatts
Collector Voltage, V_c	-30 volts
Collector Current, I_c	7 milliamperes
Collector Dissipation	210 milliwatts
Available Power Gain	18 db
Load Resistance	5000 ohms
Power Output	50 milliwatts

R. J. KIRCHER

R. M. RYDER

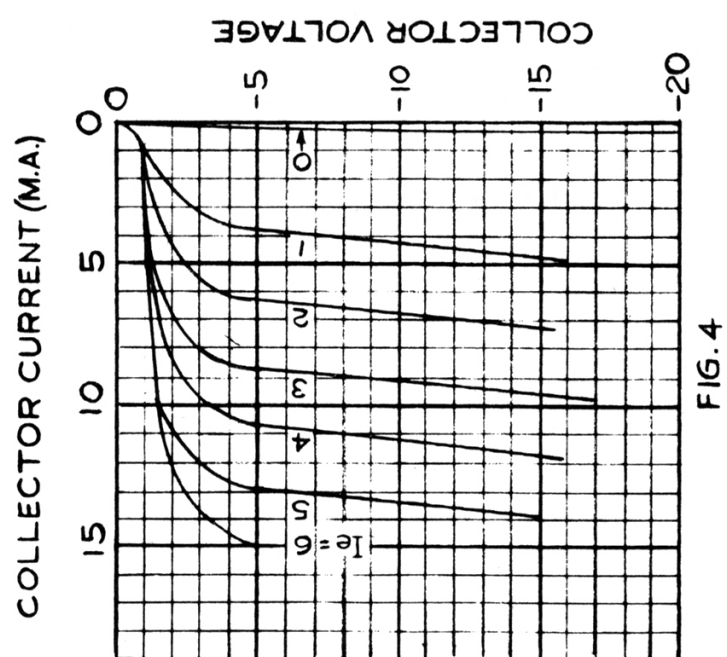
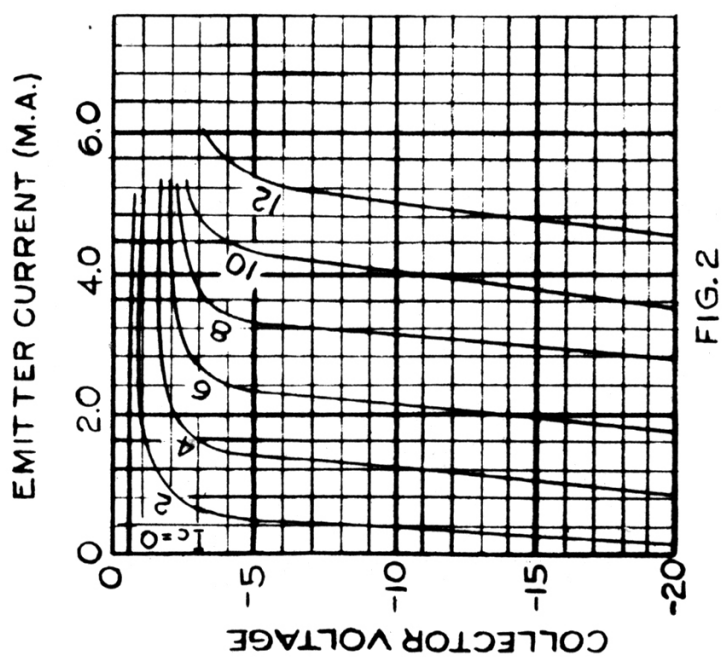
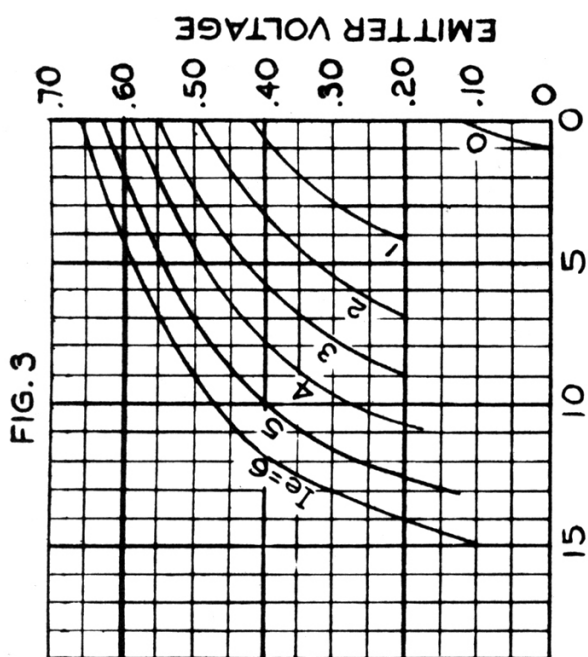
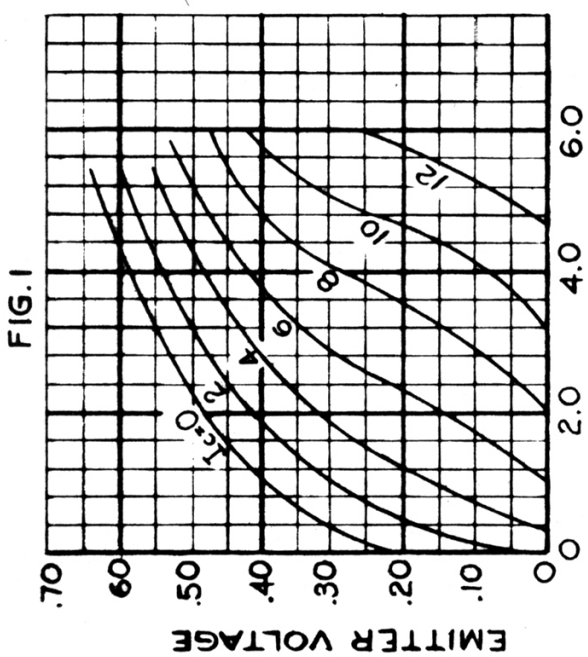
OUTLINE DRAWING OF TRANSISTOR



APPLICABLE TO
TYPE No's

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STATIC CHARACTERISTICS OF M1725 TRANSISTOR



B0 755501

STATIC CHARACTERISTICS OF M1729 TRANSISTOR

FIG. 1

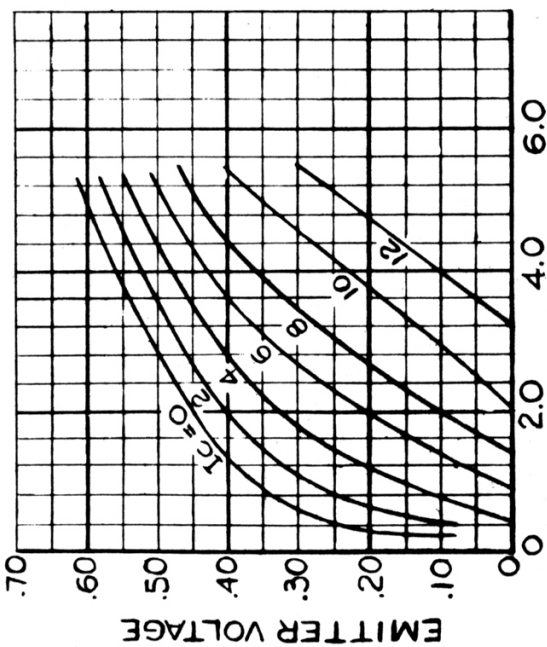
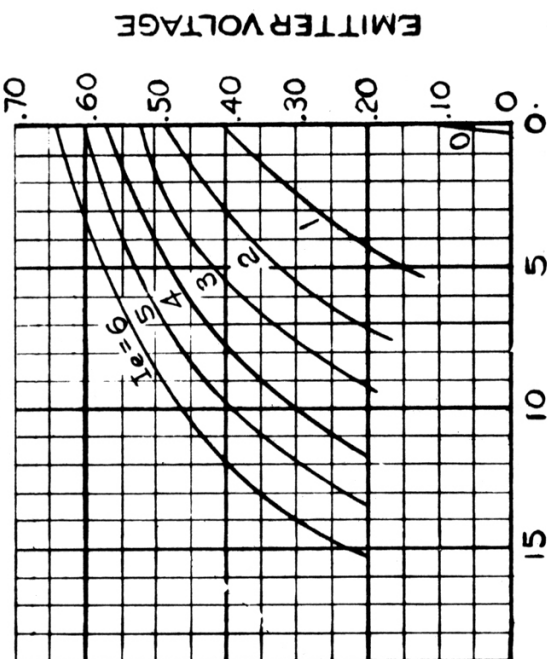


FIG. 3



EMITTER CURRENT (MA.)

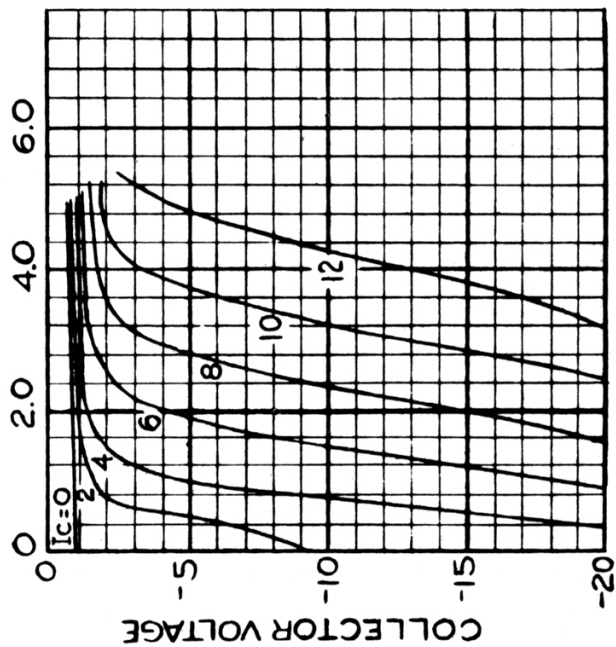


FIG. 2

COLLECTOR CURRENT (MA.)

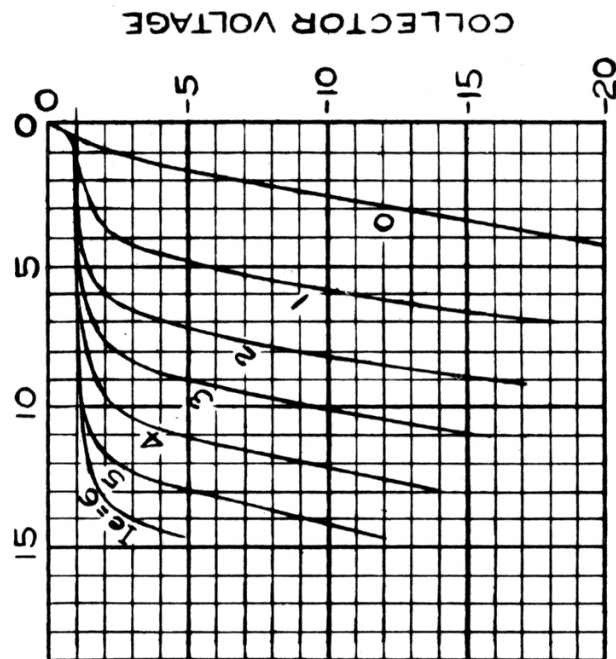


FIG. 4

B0 755502

EXPLORATORY DEVELOPMENT CHARACTERISTICS

BTL M1727 AND BTL M1728 P-N JUNCTION DIODES

The BTL M1727 and BTL M1728 P-N junction diodes, are designed for low forward impedance and high reverse impedance, respectively. Their particular advantages are low forward impedances, high reverse impedances, high back voltage capabilities, and small size. Their major limitation is comparatively low (100 KC) frequency cutoff. Summaries of the terminal characteristics of these two devices are given in the following sheets. -

BTL M1727 P-N JUNCTION DIODE

Reference: JAN-1A

Description: Germanium P-N junction diode, low forward impedance

<u>Ratings:</u>	epx	il	Io	Pp	TA
Absolute	v	mA	mA	mW	oC
Maximum	-	-	-	200 (note 1)	80
Test Conditions	-	-	-	-	25

Dimensions: as per outline Figure 15-1

Mounting position: any

Connections: red spot on shell marks positive terminal
for easy flow

BTL M1727 P-N JUNCTION DIODE - CONT.

<u>Ref.</u>	<u>Test</u>	<u>Conditions</u>	<u>Min.</u>	<u>Max.</u>
-	Handling precautions	Note 2		
F-6b(1)	Vibration	-		
F-6c(1)	Forward current	Eb = 1Vdc	Ib: 10	- mAdc
F-6c(1)	Reverse current	Eb = 40Vdc Eb = 100Vdc	Ib: - Ib: -	10 pAdc 20 pAdc
-	Reverse current	Note 3		
F-6c(1)	Reverse voltage	Ib - 100pAdc	Vx: 150	- Vdc
-	Frequency cutoff	Note 4		
-	Noise	Note 5		

BTL M1728 P-N JUNCTION DIODE

Reference: JAN-1A

Description: Germanium P-N junction diode, high back impedance

<u>Ratings:</u>	epx	il	Io	Pp	TA
Absolute	v	mA	mA	mW	°C
Maximum	-	.-	-	200 (note 1)	80
Test Conditions	-	-	-	-	25

Dimensions: as per outline Figure 15-1

Mounting position: any

Connections: redspot on shell marks positive terminal
for easy flow.

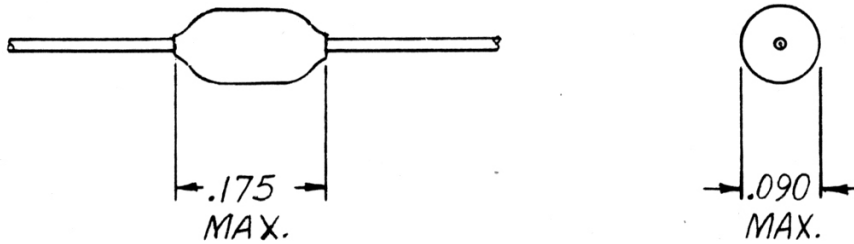
BTL M1728 P-N JUNCTION DIODE - CONT.

<u>Ref.</u>	<u>Test</u>	<u>Conditions</u>	<u>Min.</u>	<u>Max.</u>
-	Handling Precautions	Note 2		
F-6b(1)	Vibration	-		
F-6c(1)	Forward current	$E_b = 1V_{dc}$ $I_b:$	3	-mA _{dc}
F-6c(1)	Reverse current	$E_b = 100V_{dc}$ $I_b:$	-	10 μA_{dc}
F-6c(1)	Reverse current	$E_b = 200V_{dc}$ $I_b:$	-	15 μA_{dc}
F-6c(1)	Reverse current	Note 3		
F-6c(1)	Reverse voltage	$I_b = 100\mu A_{dc}$ V_x	300 -	V_{dc}
-	Frequency cutoff	Note 4		
-	Noise	Note 5		

BTL M1727 and BTL M1728

- Note 1 For ambient temperatures above 50°C the maximum dissipation rating becomes 100 mW.
- Note 2 **When** soldering to or bending the lead wires they **should** be gripped with pliers between the operation and the connections to the element.
- Note 3 At an ambient temperature of 60°C the maximum reverse leakage current ratings are 10 times higher than those given for 25°C.
- Note 4 Rectified dc output for continuous wave applications may fall off considerably in the range below 100 kc and prohibitively in the range from 100 kc to 1 MC. Step-function action in which the element is carried from reverse to forward is more rapid in response.
- Note 5 The short circuit noise current in the band from 200 cps to 200,000 cps should not exceed 10^{-7} amp rms at a dc bias of 90 v reverse.

JOHN N. SHIVE



LEAD WIRES .010 NICKEL, LENGTH $1\frac{1}{2}$ IN. MIN.

POLARITY INDICATED BY RED SPOT ON SHELL
AT POSITIVE END FOR EASY FLOW DIRECTION.

EXTERNAL DETAIL OF M-1727, M-1728, M-1754, M-1755
P-N JUNCTION DIODES.

FIG. 15-1

EXPLORATORY DEVELOPMENT CHARACTERISTICS FOR

B. T. L. M1734 TRANSISTOR

Numerous important system applications need a device combining good switching capabilities, and low voltage and power requirements with high speed operation. A transistor unit, designated the BTL M1734, is under development to exploit the possibilities of the point-contact type in these directions. Briefly, as an indication of performance, the BTL M1734 makes possible computer-type switching operations at rates of at least a megacycle per second with voltage supplies of 8-24 volts and average power drains per unit of the order of 25-50 milliwatts.

Complete specifications for the BTL M1734 have not yet been set, but development ones are attached.

A curve of current gain (α) versus frequency is taken with $V_c = -7$ v., and $I_e = 0.5$ mA. The frequency at which α has fallen to 0.707 of its low-frequency value (3 db down) is designated the frequency cutoff, f_c .

A maximum time of response at a low voltage (-7 v) is assured by requiring that $f_c \geq 10$ mc/sec.

Output or collector large signal switching characteristics are fixed by cutoff and saturation requirements. These are 1) Cutoff,

$$I_e = 0, V_c = -7; I_c \leq -0.7 \text{ ma.}$$

(This value of I_c called I_{c0})

2) Saturation:

$$I_e = 3 \text{ ma.}, I_c = -4 \text{ ma.}; V_c \leq -1.2 \text{ volts}$$

(This value of V_c called $V_{c3,4}$)

These specifications assure that a considerable proportion of a low collector supply voltage can be obtained as output voltage with low load resistances.

The cutoff input resistance is fixed by requiring that the cutoff resistance of the emitter to be greater than 100 K. at $V_e = -10$ V. Also, the large signal characteristic is held by fixing the minimum large signal current gain. This is done by introducing a 2 mA. step into the emitter (from cutoff) with -8 v. collector supply and 1000 ohm load. It is required that $\alpha \geq 1.8$ under these conditions, and as a further check on response time, this minimum value of α must be reached within 0.1 psec. or less.

SPECIFICATIONS B. T. L. M1734

Reference - JAN-1A

Description: Transistor-High Speed Switching Applications

<u>Ratings</u>	V_c	I_c	V_e	I_e	P_c	T_a	Note 1
Absolute	V	mA	V	mA	mW	°C	
Maximum	-100	-40	-40	+40	120		
Test Conditions	-	-	-	-	-	25	

Dimensions: Per Outline

Mounting Position: Any

Connections: Per Outline Fig. 14-1

<u>Ref.</u>	<u>Test</u>	<u>Conditions</u>	<u>Min.</u>	<u>Max.</u>
-	Handling Precautions	Note 2		
F-3	Aging Period	24 hrs, Note 4		
	Vibration & Shock	Note 3		
	OFF Collector Current	$V_c = -7 \text{ Vdc}; I_c:$ $I_e = 0$	0	-0.7 mAdc
	ON Collector Voltage	$I_e = 3 \text{ mA } V_c:$ $I_c = -4 \text{ mA}$	0	-1.2 Vdc
	Emitter Resistance Reverse	$V_e = -10 \text{ Vdc}; I_e:$ $I_c = 0$	0	-0.1 mAdc
	Frequency Cutoff	$I_e = 0.5 \text{ mAdc}; f_c:$ $V_c = -7 \text{ Vdc}$ Note 5	10	- mc sec.
	Alpha after 0.1 μ sec	$I_e = 2 \text{ mA } \alpha:1.8$ $V_c = -7 \text{ Vdc}$ Note 6		

- Note 1 Inward direction of current is taken as positive for both emitter and collector. Voltages are measured with respect to the base. Subscripts "c" and "e" refer to collector and emitter respectively. Voltages are taken on an absolute basis so that a voltage of $V_c = -40$ is greater than a voltage of $V_c = -30$ volts. DC rating are on the basis of any duration longer than the order of 5 μ s. Transients in excess of the rating, but with durations much less than 5 μ s, may not injure the unit; it is to be understood, however, that such service is experimental.
- Note 2 The transistor should not be subjected to service in which there may be excessive transients as in plugging in and out with power on, but this may be done if under any case the rating are not exceeded. Base contact should be made first. If solder connections are made, heat sink protection on the transistor side of the joint should be provided as with flat nose pliers. Solder connections to the base are not recommended.
- Note 3 The same degree of ruggedness experienced with germanium diodes may be expected. Transistors have been shocked and accelerated to 10,000 G with no difficulties, except, when applied in such a direction as to lift the points, there may be failure.
- Note 4 All tests should be made after aging at 100 mW collector dissipation for 24 hours.
- Note 5 Frequency at which oc , the small signal current gain, is down 3 db from its low frequency value is designated, f_c .
- Note 6 For this test, a 2 mA step function is applied to the emitter from cutoff. The collector load is 1000 ohms.

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EXPLORATORY DEVELOPMENT CHARACTERISTICS FOR B.T.L.

M1740 P-N JUNCTION PHOTOCELL ELEMENT

During the development of an encoding system the P-N junction photocell emerged as the preferred unit for use in the photodetection circuit of the angular position encoder. Reasons for this preference are: high reproducibility from unit to unit in manufacture, low dark current, low noise, and small size.

Development data sheets and specifications are attached.

DATA SHEET ON B.T.L. M1740 PHOTOCELL

Maximum ratings Not to be exceeded in continuous operation

Bias Voltage, E_{bb}	200 Vdc
Bias Current, I_b	10 mAdc
Dissipation, P_p $T < 50^\circ\text{C}$	100 mWdc
$T > 50^\circ\text{C}$	50 mWdc
Ambient Temperature, T	80°C

Nominal AC Equivalent Circuit Parameters

At operating point $E_{bb} = 90 \text{ Vdc}$;

Flux = .00625 lm*

Junction Resistance, r_j 10 megohms

Body Resistance, r_b 200 ohms

Transfer Constant, K .035 milliamps
millilumen

*Black body source at color temperature 2400°K, focussed into spot 0.5 mm in diameter on junction.

DATA SHEET ON B.T.L. M1740 PHOTOCELL - CONT.

Typical Operating Condition: Small signal photoelectric transducer, 20°C

Supply Voltage	180 Vdc
Load Resistance	.5 megohm
Light Flux, Steady Component	.006 lm
Bias Current, Ib	190 pA _{dc}
Bias Voltage, Ebb	90 Vdc
Dissipation, Pp	17 mW _{dc}

Typical Operating Conditions: Light-operated on-off switch, 20°C

Supply voltage	135Vdc	135 Vdc
Load Resistance	1 megohm	0.5 megohm
Dark Current	<20pA	<20pA
Light Flux	>.005 Im	>.009 Im
Light Current	135pA	270pA

Short Circuit Noise Current*, in 1 cycle per sec. band at 1000 cycles per sec.

Ebb = 90 Vdc; Ib = 7pA_{dc} (dark) $I_n = 2 \times 10^{-5} \text{pA}_{ac} \text{ rms}$

Ebb = 90 Vdc; Ib = 450pA_{dc} (light) $I_n = 1 \times 10^{-4} \text{pA}_{ac} \text{ rms}$

Frequency Cutoff, at which output is -3 db from low frequency value $f_{co} > 25 \text{ kc}$

Spectral Range

Approximately 75% quantum efficiency for incident light in the visible and infra red to 1.6 micron wave length. See Figure 17-2.

*The noise power per unit band approximates a $\frac{1}{f}$ relationship with frequency at which the noise is measured.

SPECIFICATIONS ON B.T.L. M1740 PHOTOCELL ELEMENT

Reference: JAN-1A

Description: photocell element - germanium p-n junction
(visible and infra-red sensitive)

Ratings:	Ebb	Light Source	Light Flux	I _b	P _p	T
Absolute	Vdc	-	lm	mAdc	mWdc	°C
Maximum	200	-	-	10	100 Note 6	80

Test Conditions: 90 Note 1 .00625 - - 20

Spectral Response: Note 3 Mounting: any position

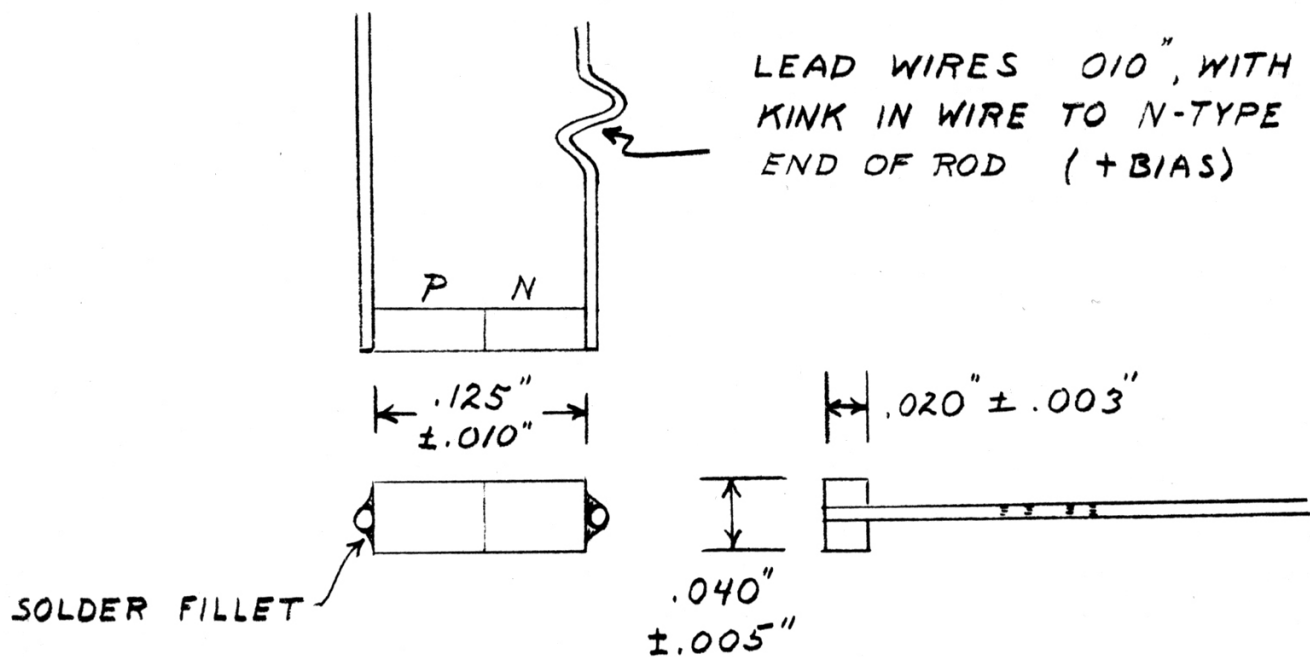
Dimensions: per outline Figure 17-1.

Connections: per outline Figure 17-1.

<u>Ref.</u>	<u>Test</u>	<u>Conditions</u>	<u>Min.</u>	<u>Max.</u>
	Handling Precautions	Note 4		
F-7d	Dark Current	T = 20°C	LIb -	20pAdc
		T = 55°C	LIb -	100pAdc
	Light Current	T = 20°C	Ib 170	- pAdc
		T = 55°C	Ib 200	- pAdc
	Frequency response	-3 db	f _{co} 25,000	- cps
	Noise Current	Note 5		

- Note 1 The testing light source is a tungsten filament operated at a color temperature of 2400° Abs.
- Note 2 This flux is focused into a small spot 1/2 mm in diameter, centered on the p-n junction tract on the .040 x .125 face of the cell element.
- Note 3 The spectral response corresponds to a quantum efficiency of approximately 75% in the region from visible blue to 1.6 microns in the infra red. See Figure 17-2.
- Note 4 The waxed surfaces of the element should not be handled. When the wires are to be bent, they should be gripped between the bend and the soldered electrodes, so as to place no stress on the latter.
- Note 5 The short-circuit noise current in the band from 200 cps to 200,000 cps should not exceed 10^{-7} ampere rms at a dc bias of 90 volts.
- Note 6 At ambient temperatures above 50°C, the maximum dissipation rating is reduced to 50mW.

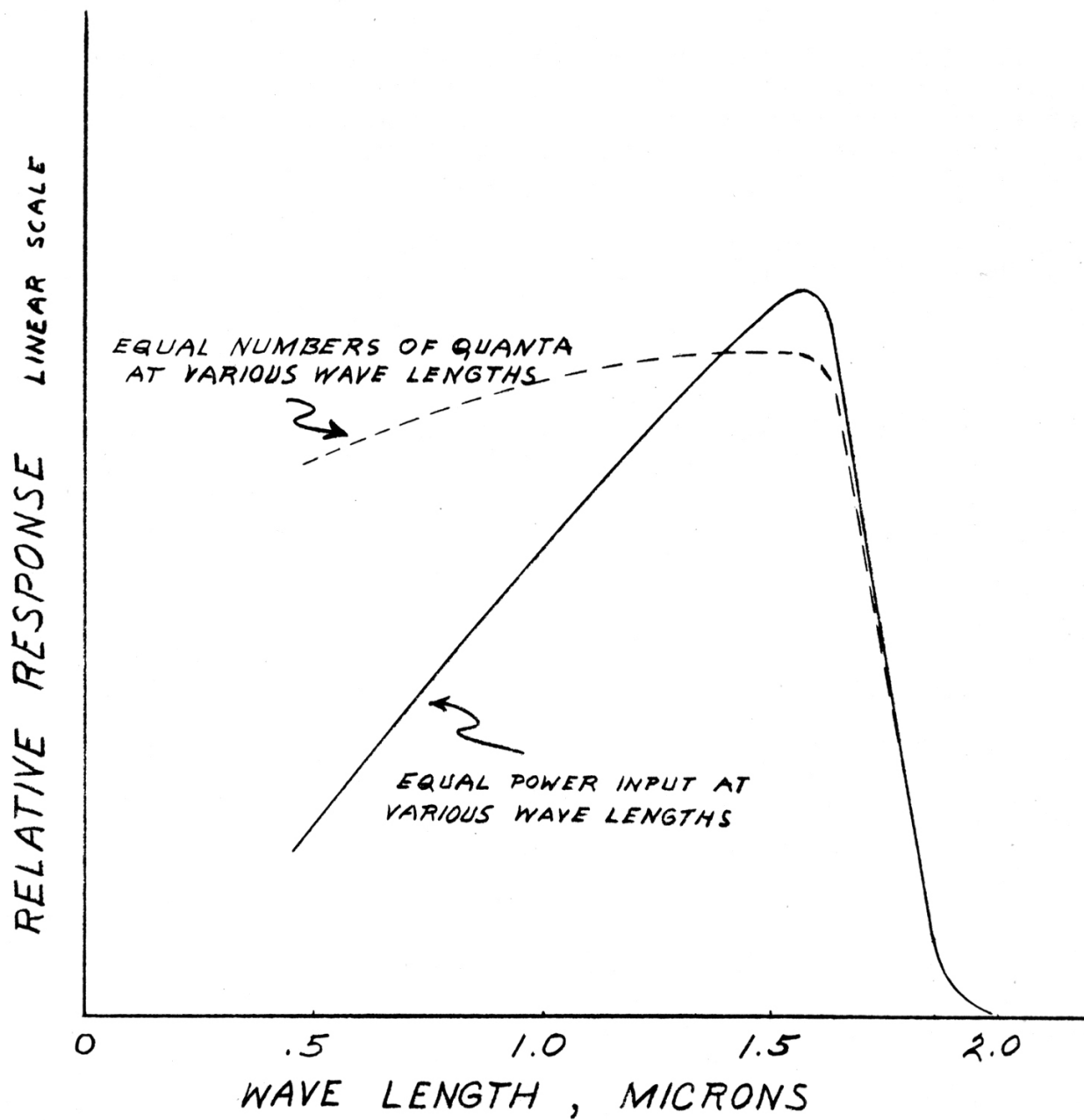
JOHN N. SHIVE



SURFACES OF ROD COVERED WITH
PROTECTIVE COAT OF WAX (NOT SHOWN)

DETAIL OF P-N JUNCTION ELEMENT

FIG. 17-1



M-1740 SPECTRAL RESPONSE

FIG. 17-2

EXPLORATORY DEVELOPMENT CHARACTERISTICS FOR THE

BTL M1752 TRANSISTOR

The BTL M1752 transistor is an NPN junction transistor which can give high power gain at high efficiency, even at very low operating voltages and currents. In addition, the noise figure of the device is very much lower than that of point contact transistors of conventional design.

A limited number of development models of the BTL M1752 have been made for preliminary study in several possible circuit applications. Figure 18-1 shows outline dimensions and lead arrangement of these models, and a development specification is attached.

SPECIFICATIONS BTL M1752 TRANSISTOR

Reference - JAN-1A

Description - Transistor

Ratings:	V _c	I _c	V _e	I _e	Load	Dissipation P _e P _c	Ambient Temp. degrees C
Units	Volts	mA	Volts	mA	ohms	milliwatts	
Maximum	+50	5		5		50	50

Test Conditions

Small Signal							
+4.5				1.0			Approx. 25

Dimensions: per Outline Dwg. Fig. 18-1

Connection: per Outline Dwg. Fig. 18-1

<u>Test</u>	<u>Conditions</u>	<u>Min.</u>	<u>Max.</u>
Handling	Note 2		
Holding Period	48 hrs., Note 5		
Vibration and Shock	Note 3		
Collector Voltage		0	+50 volts
Input Resistance		-	1000 ohms

<u>Test</u>	<u>Conditions</u>	<u>Min.</u>	<u>Max.</u>
Output Resistance		100,000	
Current Amplification Factor	2	.95	1.0

- Note 1 Subscripts c and e refer to collector and emitter respectively. Voltages are measured with respect to the base. D-c ratings are on the basis of any duration longer than about 5 microseconds. Transients of shorter duration somewhat in excess of the ratings may not injure the transistor.
- Note 2 The transistor should not be subjected to excessive transients such as may occur on plugging in or out with power on. This may be done if in any case the ratings are not exceeded; base contact should be made first.
 • When solder connections are made, heat sink protection on the transistor side of the joint should be provided, as with flat-nose pliers.
- Note 3 The same degree of ruggedness experienced with germanium diodes may be expected.
- Note 4 For ambient temperatures from 50° C up to 80° C the maximum collector dissipation should not exceed 25 milliwatts.
- Note 5 All tests should be made after holding period.
 Reference F3, JAN-1A.
- Note 6 Operating point for measurement of circuit parameters is $I_e = 1 \text{ mA}$, $V_c = + 4.5$.

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OUTLINE DRAWING OF M1752 TRANSISTOR

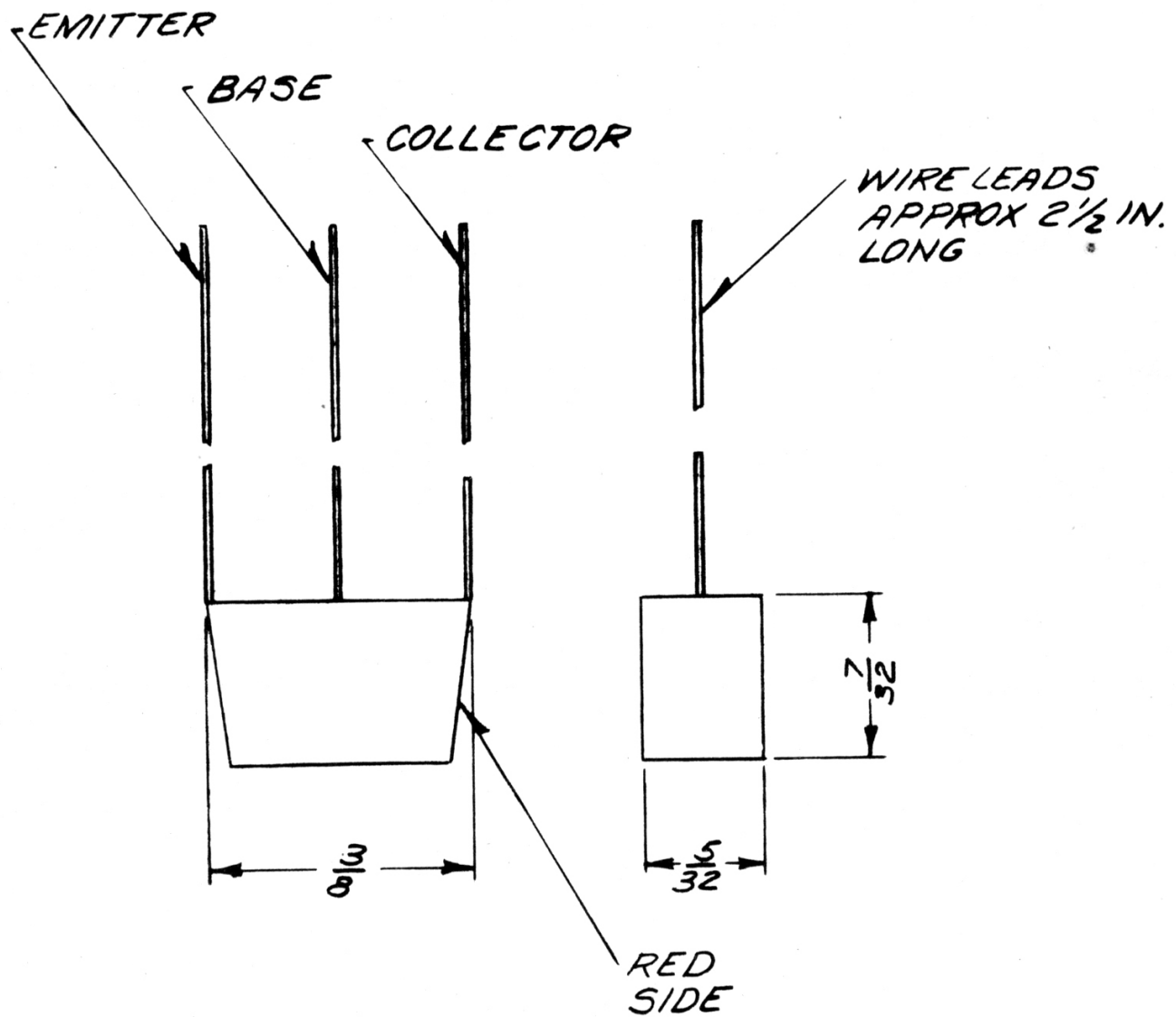


FIG. 18-1

EXPLORATORY DEVELOPMENT CHARACTERISTICS FOR

BTL M1754 and M1755 P-N JUNCTION DIODES

The BTL M1754 is a new p-n junction diode which is intended for applications where unusually high forward-to-back ratios are required in the operating range below 50 volts. It does not have a high back voltage sustaining ability in the range above 50 volts. The BTL M1755 is a p-n junction diode for which the reverse characteristic exhibits a sharp "break-away" from the saturation current and proceeds to higher current along a Zener line of rapidly decreasing impedance. We thus have a current-saturation region of several megohms a-c impedance sandwiched between the forward characteristic region and the Zener region, both of which may have a-c impedances of the order of tens of ohms.

The equation of the Zener region portion of the reverse characteristic is:

$$I = V \times 10^{(11 - \frac{10^7}{E})} \text{ amps/sw.cm.}, \text{ where } E = \frac{V}{d},$$

the field in the barrier, with d being the barrier thickness. The reciprocal of the slope of the Zener characteristic, which gives the a-c impedance in the Zener region, is:

$$Z_z = \frac{V^2}{i(V + 2.3 \times 10^7 d)} \quad \text{ohms per sq. cm.},$$

showing that this impedance is a function of the saturation voltage (which remains practically constant over this region), the current, and the barrier thickness. The properties of the barrier in this region are independent of temperature. However, the Zener region characteristic of a practical diode is temperature dependent insofar as the series resistance of the germanium body of the element is so dependent. If the diode is to be of much practical use the onset of the Zener region should occur below 100 volts in order to give a usefully long current range below the 200 mW maximum allowable dissipation point. To date Zener voltages have been found in the range from 12V up to over 100V.

For neither of these devices have enough samples been made and studied to justify the presentation here of full specifications. Accordingly there are given below only a list of those limits which have been tentatively established for measurement purposes.

M1754 TEST LIMITS

Forward current at 1 Vdc	25 mA min.
Reverse current at 25 Vdc	$.5 \times 10^{-6}$ max.
● Reverse current at 40 Vdc	1.0×10^{-6} max.
Reverse voltage at 100×10^{-6} dc	75 V min.
Power dissipation	200 mW max.

M1755 TEST LIMITS

Forward current at 1 Vdc	5 mA min.
A-c resistance in reverse current saturation region	1 megohm min.
A-c resistance at 2 mA reverse (Zener region)	1000 ohms max.
Zener limiting voltage range	to 100 V max.
Power dissipation	200 mW max.

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